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CL-PX2080 MediaDAC™ Advanced Product Information

MediaDAC™

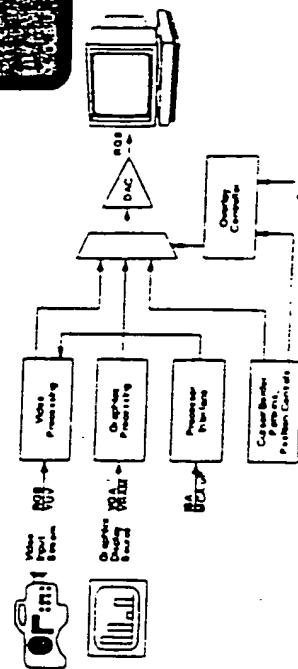
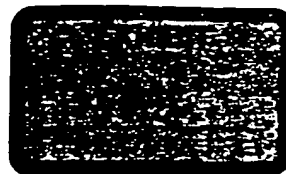
The CL-PX2080 MediaDAC™ is a multiple source, digital-to-analog video converter. It manages and mixes two different video data streams while converting the input data into the format of the display subsystem, and changes color space and resolution from the input to the output format in real time.

FEATURES

- Direct ISA/MCA bus interface
- Interlaced or non-interlaced output
- Up to 85 MHz pixel clock rates
- Video inputs
 - RGB at 60 MHz
 - RGB at 75 MHz or 85 MHz
 - RGB at 100 MHz or 110 MHz
 - RGB at 125 MHz or 135 MHz
 - RGB at 150 MHz or 165 MHz
 - RGB at 180 MHz or 195 MHz
 - RGB at 210 MHz or 225 MHz
 - RGB at 240 MHz or 255 MHz
 - RGB at 270 MHz or 285 MHz
 - RGB at 300 MHz or 315 MHz
 - RGB at 330 MHz or 345 MHz
 - RGB at 360 MHz or 375 MHz
 - RGB at 390 MHz or 405 MHz
 - RGB at 420 MHz or 435 MHz
 - RGB at 450 MHz or 465 MHz
 - RGB at 480 MHz or 495 MHz
 - RGB at 510 MHz or 525 MHz
 - RGB at 540 MHz or 555 MHz
 - RGB at 570 MHz or 585 MHz
 - RGB at 600 MHz or 615 MHz
 - RGB at 630 MHz or 645 MHz
 - RGB at 660 MHz or 675 MHz
 - RGB at 690 MHz or 705 MHz
 - RGB at 720 MHz or 735 MHz
 - RGB at 750 MHz or 765 MHz
 - RGB at 780 MHz or 795 MHz
 - RGB at 810 MHz or 825 MHz
 - RGB at 840 MHz or 855 MHz
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 - RGB at 9780 MHz or 9795 MHz
 - RGB at 9810 MHz or 9825 MHz
 - RGB at 9840 MHz or 9855 MHz
 - RGB at 9870 MHz or 9885 MHz
 - RGB at 9900 MHz or 9915 MHz
 - RGB at 9930 MHz or 9945 MHz
 - RGB at 9960 MHz or 9975 MHz
 - RGB at 9990 MHz or 10005 MHz
- Zoom controls
- Hardware cursor controls
- Three overlay combination controls
 - Input chroma color key
 - Graphics overlay color key
 - UV window

YUV
R G B

what is
for RGB
YUV + R G B
or is R G B



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DEPOSITION
EXHIBIT

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Pixel Semiconductor

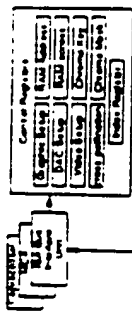
ARCHITECTURAL OVERVIEW

The CLPX2000 is a high performance, low cost, 2D/3D graphics controller. The CLPX2000 has a video port for VCR/DVR, RGB data and a graphics port with both 8 bit VCR and 12 bit high resolution ports. Its display function requires:

- 32-bit color
- Display of true color, RGB data, or 12-bit color
- Hardware cursor position and zoom
- A combination of these graphics overlay functions

Host System Interface

The CLPX2000 connects directly to ISA and VLB buses, internally decoding a 16-bit address and providing an 8-bit peripheral. Its internal ISA bus interface allows most of the controller's circuitry common to many personal computer or system expansion boards.

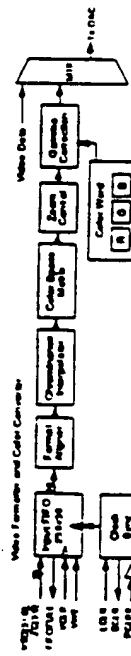


Video Frame Buffer Interface

The CLPX2000 accepts data from the graphics display source through either of two paths:

- an 8-bit VCR data path, or
- a 32-bit VRAM serial data path.

Both paths allow CLPX2000 based, next generation PC graphics subsystems to maintain compat-



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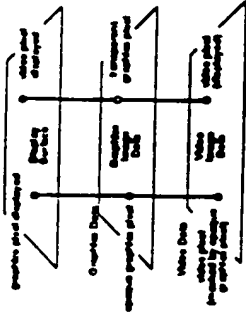
CLPX2000 MicroDAC™

- designed to accept data from VRAM serial ports, can be used with a variety of architectures
- VCR Interface
- True color (CLUT bypass) option

Graphics Overlay Control

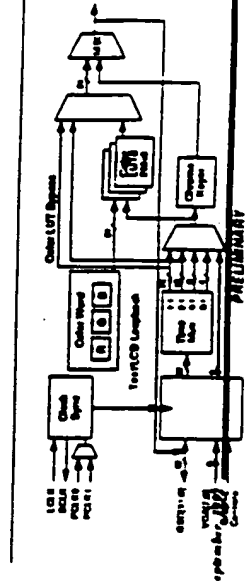
The graphics overlay controls allow a video image and a graphics image to be combined using a variety of operations (see figure right).

Every graphics pixel is either transparent or opaque. The color information for an opaque pixel is displayed on the screen. The color information for a transparent pixel is not displayed. Instead, the color information of the video pixel behind it is displayed on the screen. The graphics overlay controls determine which graphics pixels are transparent. The CLPX2000 has 256 possible overlay combinations based on the video pixel's bit, the graphics pixel's overlay color, and the XY window of the video data.



Power Down Mode

During the CLPX2000's power down condition, the DACs power down and the RAM enters a low-power, data-retaining standby mode. The process



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are carried from memory to the DAC as long as the program is running. The DAC automatically begins updating processor registers and shut down when program access is completed. The three DAC command registers are also available.

SOFTWARE SUPPORT

Cirrus Semiconductor provides a complete solution for computer based video. Numerous software support is available to ensure a quick product development cycle that keeps up with today's fast time to market requirements.

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The Company

Cirrus Logic, Inc., is a leading supplier of high integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state of the art software and firmware to complement its product lines. Cirrus Logic technology is used in leading edge personal computers, engineering workstations, and office automation.

Pirel Semiconductor, Inc., a subsidiary of Cirrus Logic, Inc., is a developer of integrated circuits for advanced display systems. These circuits enable the integration of real-time video with traditional computer graphics.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Tell to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

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1. PIN INFORMATION

The CL-PX2080 MediaDAC™ is available in a 180-pin Plastic Quad Flat Pack (PQFP) device that can be configured for ISA, MCA or Coprocessor bus implementation.

1.1 Pin Diagrams

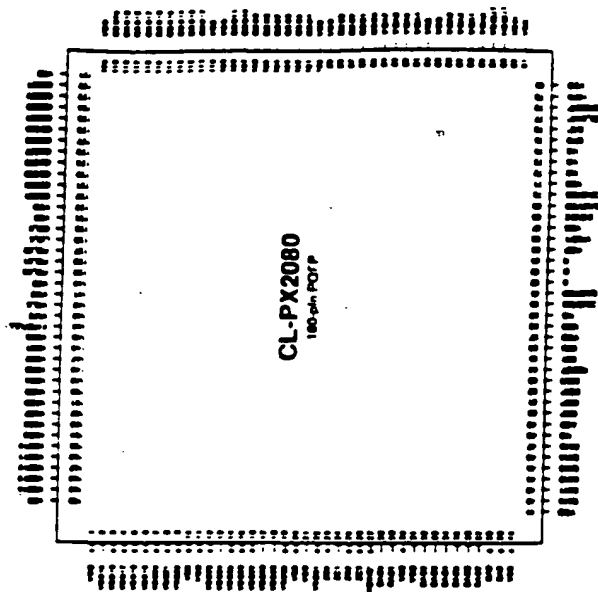


Figure 1-1. Pin Diagram — ISA Bus Configuration

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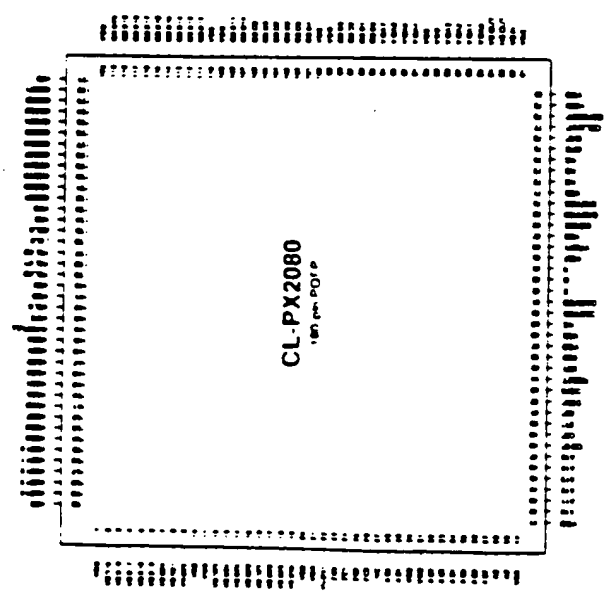


Figure 1.2. Pin Diagram — MCA Bus Configuration

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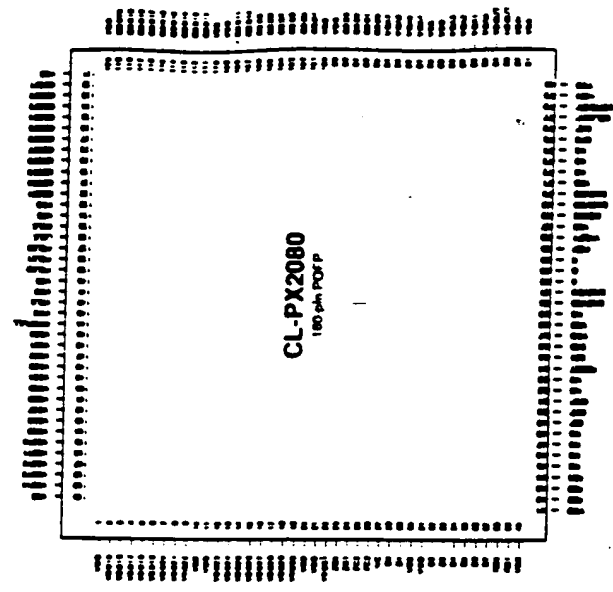


Figure 1.3. Pin Diagram — Coprocessor Bus Configuration

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12 Pin Assignment Table

The following conventions are used in the pin assignment table:

- 1 - Input
- 0 - Output
- AV - Analog signal
- PV - Periodic output
- PM - Pulse
- CM - CMOS
- CMOS - The pad has standard TTL input threshold and TTL output levels
- DS - Drive rate TTL drive capability
- OD - Open drain, TTL levels
- 4 - 4 mA sink and 2 mA source drive capability
- 12 - 12 mA sink and 4 mA source drive capability
- 24 - 24 mA sink and 8 mA source drive capability

NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE - ISA BUS MODE SUMMARY				
ADP0	41, 42, 39, 38	1	11	CMOS Address High Byte
ADP1	37, 32, 29, 28	1	11	CMOS Address and Data Low Byte
ADP2	31, 30, 27, 26	1	11	IO Read
ADP3	25, 24, 21, 20	1	11	IO Write
ADP4	19, 18, 15, 14	1	11	Address Enable
ADP5	13, 12, 9, 8	1	11	Reset
ADP6	7, 6, 3, 2	0	OD 11, 24	No Wait State
ADP7	1, 0	0	11, 8	Data Buffer Enable
ADP8	33, 32, 29, 28	0	11, 8	Data Buffer Direction
ADP9	25, 24, 21, 20	0	11	Bus Stab
ADP10	19, 18, 15, 14	0	11	Bit alternate address select
ADP11	13, 12, 9, 8	0	11	No Connect (must be left floating)
ADP12	7, 6, 3, 2	0	11	No Connect (must be left floating)
ADP13	1, 0	0	11	No Connect (must be left floating)
PROCESSOR INTERFACE - MCA BUS MODE SUMMARY				
ADP14	41, 42, 39, 38	1	11	CPU Address High Byte
ADP15	37, 32, 29, 28	1	11	CPU Address and Data Low Byte
ADP16	25, 24, 21, 20	1	11	No Connect (must be left floating)
ADP17	19, 18, 15, 14	1	11	Command
ADP18	13, 12, 9, 8	1	11	Memory or IO Cycle
ADP19	7, 6, 3, 2	1	11	Status 0
ADP20	1, 0	1	11	Reset
ADP21	33, 32, 29, 28	0	OD 11, 8	Data Buffer Enable
ADP22	25, 24, 21, 20	0	OD 11, 8	Data Buffer Direction
ADP23	19, 18, 15, 14	0	11	Bus Stab
ADP24	13, 12, 9, 8	0	11	Bit alternate address select
ADP25	7, 6, 3, 2	0	11	No Connect (must be left floating)
ADP26	1, 0	0	11	No Connect (must be left floating)

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12 Pin Assignment Table

The following conventions are used in the pin assignment table:

- 1 - Input
- 0 - Output
- AV - Analog signal
- PV - Periodic output
- PM - Pulse
- CM - CMOS
- CMOS - The pad has standard TTL input threshold and TTL output levels
- DS - Drive rate TTL drive capability
- OD - Open drain, TTL levels
- 4 - 4 mA sink and 2 mA source drive capability
- 12 - 12 mA sink and 4 mA source drive capability
- 24 - 24 mA sink and 8 mA source drive capability

NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE - COPROCESSOR BUS MODE SUMMARY				
ADP0	44, 42, 39, 38	1	11	Register Select
ADP1	37, 32, 29, 28	1	11	Data
ADP2	31, 30, 27, 26	1	11	IO Read Cycle
ADP3	25, 24, 21, 20	1	11	IO Write Cycle
ADP4	19, 18, 15, 14	1	11	Reset
ADP5	13, 12, 9, 8	1	11	Chip Select
ADP6	7, 6, 3, 2	1	11	Bus Stab
ADP7	1, 0	1	11	No Connect (must be left floating)
ADP8	33, 32, 29, 28	1	11	No Connect (must be left floating)
ADP9	25, 24, 21, 20	1	11	No Connect (must be left floating)
ADP10	19, 18, 15, 14	1	11	No Connect (must be left floating)
ADP11	13, 12, 9, 8	1	11	No Connect (must be left floating)
ADP12	7, 6, 3, 2	1	11	No Connect (must be left floating)
ADP13	1, 0	1	11	No Connect (must be left floating)
GRAPHICS PORT INTERFACE				
ADP14	122, 121, 119, 118	1	33, 8	Graphics Source Data
ADP15	109, 101, 88, 85	1	11	VGA Graphics Source Data
ADP16	84, 81, 80, 85	1	11	Pixel Input Clock 0
ADP17	136	1	11	Pixel Input Clock 1
ADP18	135	1	11	Latch Clock Input
ADP19	134	1	11	VRAM Shift Clock Output
ADP20	133	0	11, 12	Odd Even Field Input
ADP21	132	0	11	Graphics Port Select
ADP22	131	0	11	Active Display Enable
ADP23	130	0	11	Composite Blank Input
ADP24	129	0	11	Vertical Sync Input
ADP25	128	0	11	Horizontal Sync Input
ADP26	127	0	11, 8	Vertical Sync Output
ADP27	126	0	11, 8	Horizontal Sync Output
ADP28	125	0	11, 12	Pixel Clock Output
VIDEO PORT INTERFACE				
ADP29	124, 123, 122, 121	1	11	Video Source Data
ADP30	120, 119, 118, 117	1	11	Zoom Control Code
ADP31	116, 115	1	11	FPO Full Indication
ADP32	114	1	11	Video Clock Input
ADP33	113	1	11	Video FPO Write Enable



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NAME	Pin	Type	Cell	FUNCTION
MONITOR INTERFACE				
R	84	O	AN	Analog Red
G	81	O	AN	Analog Green
B	82	O	AN	Analog Blue
REF	83	I	AN	Current Reference
SENSE	88	O	TTL, 8	Monitor Sense
VREF	86	O	AN	Voltage Reference 1
POWER INTERFACE				
VDD	1, 11, 21, 31, 41, 51, 61, 71, 81, 91, 101, 111, 121, 131, 141, 151, 161	PWR		+5 VDC for Digital Logic and Interface Buffers
VSS	10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160	PWR		Ground for Digital Logic and Interface Buffers
DACVDD	81, 88	PWR		+5 VDC for DAC
DACVSS	80, 70	PWR		Ground for DAC
NO CONNECTS				
NC	72	N/A	N/A	No Connect (must be left floating)
NC	73	N/A	N/A	No Connect (must be left floating)
NC	74	N/A	N/A	No Connect (must be left floating)

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2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface - ISA Bus Mode

Signal	Pin	Type	Cell	Function
SA[15:0]	47, 42, 36, 38	I	TTL	CPU Address High Byte: SA[15:0] specify the resource to be accessed during an IO or memory cycle.
SAQ[7:0]	31, 32, 29, 28	IO	SS, 17	CPU Address and Data Low Byte: The lower byte of address is multiplexed with low byte of data externally to transfer data to and from the CL-PX1000 during an IO cycle.
IOR*	60	I	TTL	IO Read: The active low input signal indicates an IO read cycle.
IOW*	61	I	TTL	IO Write: The active low input signal indicates an IO write cycle.
ARM	46	I	TTL	Address Enable: The active high input signal indicates a DMA cycle is in progress.
RESET	64	I	TTL	Reset: The active high input signal indicates that the CL-PX1000 is to cease all activity and perform a hardware reset.
HDWS*	27	O	OD, TTL, 24	No Wait State: This open drain output specifies that the host should run a new wait state cycle. The default ISA bus cycle is one wait state.
DEN*	62	O	TTL, 8	Data Buffer Enable: The open drain output, when pulled low, enables the host data bus buffer.
DDR	63	O	TTL, 8	Data Buffer Direction: The open drain output specifies the direction of data flow on bus SAQ[15:0]. A high level indicates that the host system is driving data to SAQ[15:0] (write cycle), and a low level indicates that the CL-PX1000 is driving SAQ[15:0] (read cycle) to the host system.
BS[1:0]	55, 56	I	TTL	Bus Select: These two bits indicate the bus mode selected for the operation of the CL-PX1000. 0 0 ISA bus mode 0 1 MCA bus mode 1 0 Local hardware interface mode
ALT	66	I	TTL	Alternate address select: Enables secondary ISA address range for B/R access. 0 Primary ISA address range 1 Secondary ISA address range
NC	48	N/A	N/A	No Connect (must be left floating)



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2.3 Processor Interface - MCA Bus Mode

Signal	Pin	Type	Cell	Function
AI[15:0]	47-62	I	TTL	CPU Address High Byte: AI[15:0] over the bus to be accessed during an I/O or memory cycle.
AI[7:0]	37-42	I/O	5V, 12	CPU Address and Data Low Byte: AI[7:0] is multiplexed with data externally to handle data to and from the CL-PX2000 during an I/O cycle.
MC	27	MA	MA	No Connect (must be left floating)
CM[0]	48	I	TTL	Command: This active low input signal indicates when data is on bus AI[15:0] during a write cycle, and that the CL-PX2000 should place valid data on the bus during a read cycle.
MD[0]	48	I	TTL	Memory or I/O Cycle: This active low signal indicates when 31' and 30' is ready for current bus cycle.
				MD[0] 30' 31'
				0 0 0 Reserved
				0 0 1 I/O Write
				0 1 0 I/O Read
				0 1 1 I/O Active
				1 0 0 Reserved
				1 0 1 Memory Write
				1 1 0 Memory Read
				1 1 1 I/O Active
51'	50	I	TTL	Strobe 1: This active low signal works with MD[0] and MD[1] to strobe the current bus cycle (see table under MD[0]).
50'	51	I	TTL	Strobe 0: This active low signal works with MD[0] and 51' to strobe the current bus cycle (see table under MD[0]).
CDRESET	54	I	TTL	Reset: This active high input signal indicates that the CL-PX2000 is to come out of active and perform a hardware reset.
DEW	52	O	OD, TTL, 8	Data Buffer Enable: This open drain output, when pulled low, enables the host data bus buffer.
DDR	53	O	OD, TTL, 8	Data Buffer Direction: Indicates the direction of data flow on bus SMD[15:0]. A high level indicates that the host system is driving data to SMD[15:0] (write cycle), and a low level indicates that the CL-PX2000 is driving SMD[15:0] (read cycle) to the host system.
BS[1:0]	55-56	I	TTL	Bus Select: These two bits indicate the bus mode selected for the operation of the CL-PX2000.
				0 0 ISA bus mode
				0 1 MCA bus mode
				1 0 Local hardware interface mode

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2.3 Processor Interface - Coprocessor Bus Mode

Signal	Pin	Type	Cell	Function
ALT	50	I	TTL	Alternate address select: Enables secondary ISA address range for I/O access. 0 Primary ISA address range 1 Secondary ISA address range
RS[1:0]	44-47	I	TTL	Register Select: RS[1:0] specify the internal register to be accessed during a CL-PX2000 I/O cycle.
DT[0]	37-42	I/O	5V, 12	Data: DT[0] is an active high bidirectional data bus used to access the internal control registers.
DIR	50	I	TTL	I/O Read Cycle: This active low input signal indicates an I/O read cycle.
IOW	51	I	TTL	I/O Write Cycle: This active low input signal indicates an I/O write cycle.
RESET	54	I	TTL	Reset: This active high input signal indicates that the CL-PX2000 is to come out of active and perform a hardware reset.
CS	49	I	TTL	Chip Select: This active low input signal indicates that the CL-PX2000 is being accessed by the host system.
BS[1:0]	55-56	I	TTL	Bus Select: These two bits indicate the bus mode selected for the operation of the CL-PX2000.
				0 0 ISA bus mode
				0 1 MCA bus mode
				1 0 Local hardware interface mode
MC	53-52	MA	MA	No Connect (must be left floating)
MC	48	MA	MA	No Connect (must be left floating)
MC	47-46	MA	MA	No Connect (must be left floating)
MC	27	MA	MA	No Connect (must be left floating)

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2.5 Video Port Interface

Signal	Pin	Type	Cell	Function
VSYN11M	27	I	TTL	Video Source Data: Video data inputs to the CL-PX2080 through VSYN11M. The CL-PX2080 supports the following formats in both triggered and untriggered modes: 16 bit YUV (4:2:2), 16 bit RGB (4:4:4), 24 bit RGB (8:8:8). VCLK handles 16 bit modes as 2 bits per pixel word.
ZCLKM	28, 29	I	TTL	Zoom Control: ZCLKM specifies several attributes for Interpolation and alignment of the input video stream on VSYN11M when used with CL-PX2080.
F80411L	142	O	TTL	F80411L indicates when a full 8 condition occurs in the F80411L output. It is asserted low when a full 8 condition occurs in the F80411L output. It is asserted low when a full 8 condition occurs in the F80411L output. It is asserted low when a full 8 condition occurs in the F80411L output.
VCLKM	143	I	TTL	Video Clock Input: The rising edge of VCLKM is used to sample VSYN11M and ZCLKM data into the CL-PX2080 input video FIFO. VCLKM is high. VCLKM is generated by the source video processor.
VREF	144	I	TTL	Video FIFO Write Enable: VREF is asserted high data is written on the rising edge of VCLKM. VREF is asserted low when data is disabled.

2.6 Monitor Interface

Signal	Pin	Type	Cell	Function
R	64	O	AN	Analog Red: R is the analog red channel from the 8 bit digital to analog converter.
G	65	O	AN	Analog Green: G is the analog green channel from the 8 bit digital to analog converter.
B	66	O	AN	Analog Blue: B is the analog blue channel from the 8 bit digital to analog converter.
IREF	67	I	AN	Current Reference: IREF is the required 8 mA reference current for the DAC.
SENSE	68	O	TTL	Monitor Sense: Three level detecting comparators individually monitor the red, green, and blue DAC outputs. A minimum analog DAC output level generates a high-level comparator output. A minimum analog level produces a low-level comparator output. SENSE is a digital OR of the comparator outputs.
VREF1	69	O	AN	Voltage Reference 1:

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2.7 Power

Signal	Pin	Type	Cell	Function
VDD	1, 11, 21, 31, 41, 87, 90, 98, 99, 100, 120, 122, 141	PWR		+5 VDC for Digital Logic and Interface Buffers: Each VDD pin must be connected directly to the VDD plane.
VSS	10, 20, 30, 40, 54, 67, 71, 81, 90, 100, 110, 121, 124, 140, 180	PWR		Ground for Digital Logic and Interface Buffers: Each VSS pin must be connected directly to the ground plane.
DACVDD	61, 69	PWR		+5 VDC for DAC1. DACVDD must be decoupled from digital VDD with a ferrite bead or inductor.
DACVSS	60, 70	PWR		Ground for DAC1. DACVSS must be connected to the analog ground plane.

2.8 No Connects

Signal	Pin	Type	Cell	Function
NC	72	N/A	N/A	No Connect (must be left floating)
NC	73	N/A	N/A	No Connect (must be left floating)
NC	74	N/A	N/A	No Connect (must be left floating)

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3. FUNCTIONAL DESCRIPTION

The C1 P12080 MatrixDAC™ is a multi source digital to analog video converter that can manage and mix two separate raster streams that have different color spaces and resolutions. As shown in the functional block diagram in figure 3, the C1 P12080 has three input ports.

- a video input port for YUV or RGB data, and
 - two digital input ports for 8 bit VGA or 32 bit high resolution graphics
- The output to monitor can be pseudocolor or true color RGB. The video processing functions of the CI are a 2000 Mediatek include:
- format alignment,
 - chrominance interpolation
 - color space conversion
 - zoom and
 - gamma correction

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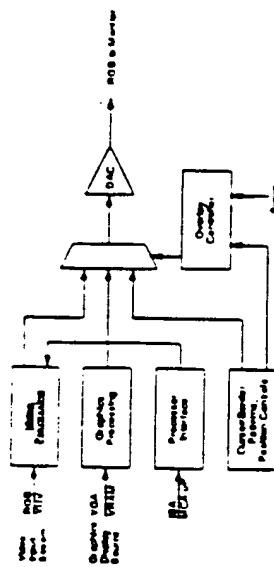


Figure 3-1. C1.PX2080MediaDAC™ Functional Block Diagram



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Figure 3 2 shows a more detailed CL-PX200 MediaDAC™ block diagram.

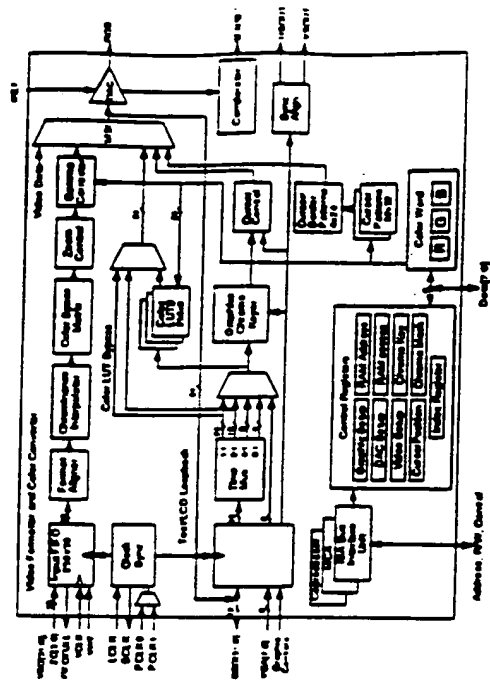


Figure 3-2. CL-P1200MedDAC™ Detailed Block Diagram

The primary functions of the MediciDAC™ include:

- Host Bus Interface
- Video Input Processing
- Graphics Frame Buffer Interface And Processing

These functions are described in the following sections. For additional detail concerning specific CL-IPX 2060 registers, refer to Section 4.



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3.1 Host Bus Interface

- The CL-PX2000 interfaces with three bus protocols:
- Industry Standard Architecture (ISA) bus
- Micro Channel Architecture (MCA) bus and
- Local hardware interface

As shown in Table 3.1 on page 29, the bus interface signals share a common set of I/O pins for a common pin assignment table (see Table 3.2 on page 30).

Table 3.1 Host System Bus I/O Pins

Pin	ISA Interface	MCA Interface	Local Hardware Interface
27	WEN	NC	NC
17, 22, 29, 24	SA[17:0]	AD[17:0]	DI[0]
16, 43	SA[15:16]	AD[15:16]	NC
14, 42, 39, 38	SA[12:13]	AD[12:13]	BS[0]
48	NC	CMD	NC
49	RTN	W/O	CS
50	OR	S1	DR
51	OW	S0	ROW
52	REN	REN	NC
53	ODIR	ODIR	NC
54	RESET	CORESET	RESET
15, 34	BS[1:0]	BS[1:0]	BS[1:0]
55	ALT	ALT	NC

The CL-PX2000 connects directly to the ISA and MCA Buses. Internally decoding a 16-bit address and responding to an 8-bit peripheral. An index and data register pair provide access to the internal registers in local hardware interface mode. The address range is externally decoded to drive the CS pin, with RS[0] selecting individual CL-PX2000 registers. Bus Selection pins BS[1:0] specify the host bus interface as shown in Table 3.2 on page 30.



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Table 3.2 Bus Selection Pins

BS[1:0]	Bus Selected
00	ISA Bus
01	MCA Bus
10	Compressor Bus
11	Reserved

The following sections describe the configuration method for each bus.

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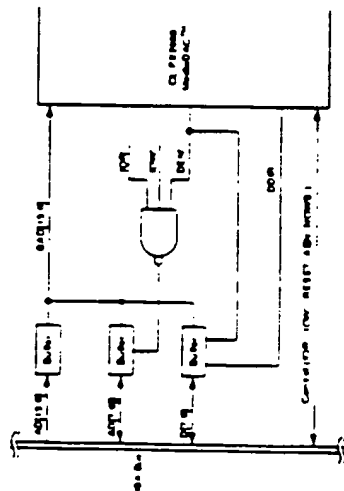


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3.1.1 ISA BUS Interface

The CL-P12080 interfaces with an ISA bus using the pin-out in the Pin Assignment Table on page 17 to support IO read and write cycles. Since the I/O of the address and the data pins are multiplexed, a tri-state buffer is required to be shown in Figure 3.3 is required to prevent contention between address and data bus.



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Figure 3.3 Example ISA Interface Circuit

Although the ISA bus supports both memory mapped and IO mapped cycles, the CL-P12080 responds only to IO mapped bus cycles. Figure 3.4 shows a typical ISA 8-bit IO cycle, illustrating both the similarities and differences in the read and write cycles.

The following is the sequence of events for a read cycle:

1. A valid address within the address range of the CL-P12080 stabilizes on the address bus. The CL-P12080 decodes the address and asserts \overline{NOWS} .
2. On the falling edge of \overline{BCLK} in T_2 , the system samples \overline{NOWS} and asserts \overline{IOR} . Asserting \overline{IOR} causes the following:
 - a. the CL-P12080 latches the address on $SA[15:0]$ and $AD[7:0]$ on the falling edge of \overline{IOR} ;
 - b. the IO buffers of $AD[7:0]$ change from input to output mode;
 - c. \overline{DDIR} goes low, using the external buffers to output to the ISA bus;

1. ISA systems have widely varying timing. Any design should include a careful analysis considering the timing specifications for the CL-P12080. See Section 6.2 on page 82 for additional information.
2. The circuit should be designed to disable the bus type address buffer on \overline{IOR} assertion.

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- d. \overline{DEN} is asserted, disabling the address buffers and enabling the data buffers.
3. After the appropriate time interval, the system negates \overline{IOR} and latches the data from the ISA bus.
4. \overline{DDIR} goes high.
5. \overline{DEN} is negated.
6. The IO buffers of $AD[7:0]$ change from output to input mode.

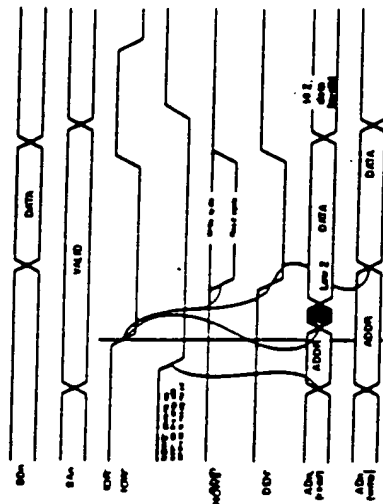


Figure 3.4 ISA 8-bit IO Cycle



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3.1.7 MCA BUS Interface

The CL-PX2000 supports 10 read and 10 write cycles to the MCA environment. The connection of the MCA bus to the CL-PX2000 is shown in Figure 3.3 on page 31. (See Section 3.2 on page 31 for additional information.) Refer to the detailed signal description on page 31 for the MCA bus cycle timing performed for signals MIO*, SD*, and ST*.

3.1.7.1 MCA IO Read

Figure 3.3 shows a typical MCA 8-bit IO cycle. The CL-PX2000 latches the address present on A[15:9] and AD[7:0] on the rising edge of AD*. During read operations, the CL-PX2000 provides valid data on the A[7:0] bus before the rising edge of CS*. The CL-PX2000 outputs the data fast enough so that no wait states are required. CS* normally is pulled high in the MCA environment, and does not need to be driven by the CL-PX2000. Since the CL-PX2000 is an 8-bit device, the MCA environment does not require it to drive the CDS18* signal.

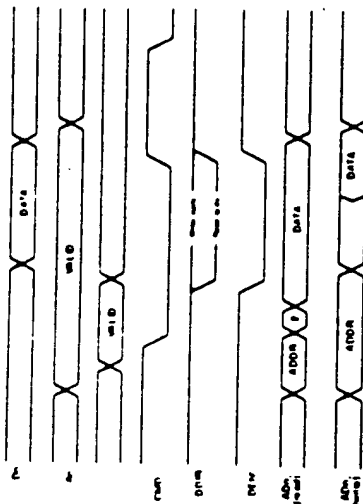


Figure 3.3 MCA 8-bit IO Cycle

3.1.3 Local Hardware Interface

The local hardware interface is a high-speed, byte-wide interface that provides the CL-PX2000 programming interface by controlling the timing of reads and writes to the CL-PX2000 in a manner similar to a static RAM. The interface has four components, which determine the read and write operations of the local hardware interface, as described in the following paragraphs:

- an 8-bit, bidirectional data bus,
- chip select input signal (CS*), which is driven by an external address decoder,
- signals RS[0:0] which select the register to be accessed, and are typically connected to the lower five

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bits of the processor address bus:

- control pins RD* and WR*, which define read and write cycles.

3.1.3.1 Local Access Cycle

A read from the CL-PX2000 occurs when CS* and RD* are low. Data from the addressed control register is placed on DT[0:7], where it may be sampled by the host between the minimum specified access time (Section 3.5 on page 31) and the rising edge of RD*.

A write occurs when CS* and WR* are low. The host system asserts CS* after RS[0:0] are stable, then asserts WR*. Data must be valid for the specified setup and hold times relative to the rising edge of WR*. Figure 3.8 shows the timing of a local hardware access.

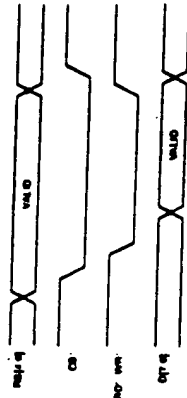


Figure 3.8 Local Hardware Interface, Cycle Timing

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3.2 Video Input Processing

The video input data bus has a 36-bit data bus, selected to as the video port. The four most significant bits of the data bus are used to select the video input format. The CL 42001 for X format operation. The remaining 32 bits of the video port may contain up to eight pixels, depending on the input format. The CL 42001 supports both tagged and untagged versions of 4:2:2 YUV, 4:4:4 RGB, and 4:4:4 RGB. The bit-mapping of these formats onto VSD[31:0] is shown in Table 3.3 on page 36. The processing of the incoming video stream is shown in Figure 3.8 on page 36 and detailed in the sections that follow.

3.2.1 Video Input FIFO

Video port data is buffered into the CL 42001 independent of the graphics data. The CL 42001 buffers video port data on the rising edge of VCLK. When the video input is 0 (VU), 8) lag goes active. If 0 (VU) lags before the VCLK rising edge, the video port data must be stable before and after the rising edge of VCLK. The video input FIFO is 256 double pixel deep.

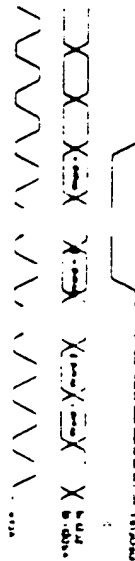


Figure 3.7 Video Input Timing

The Video Input FIFO supports 24-bit RGB color data (S 1:1) must at up to 40 MHz pixel rates, 16-bit RGB (S 2:1) must at up to 80 MHz pixel rates, and 18-bit YUV (S 2:1) must at up to 80 MHz pixel rates. The remaining video processing elements described in this section convert a variety of input formats into linear RGB and are as follows:

- Format Aligner
- Chrominance Interpolator
- Zoom Control
- Color Space Mapper
- Gamma Corrector

CL 42001

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These processing elements operate in sequence as shown in Figure 3.8. Any stage which is not needed for a specific application can be bypassed using internal control registers.

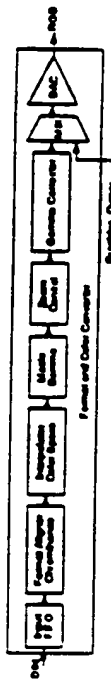


Figure 3.8 Video Input Processing Elements

3.2.2 Format Aligner

The Format Aligner accepts pixel input (VSD[31:0]) for various pixel formats described in the table below and converts it to 4:4:4 format. 1 YUV or RGB component per pixel clock. For formats requiring less than or equal to 18 bits per pixel, 2 pixels are packed into the 32-bit pixel word. VSD[31:0] pipeline registers are used to reformat data before it is passed into the color conversion circuitry. The reformatting is based on alignment to resultant 8-bit pixel values where bit 7 is the MSB. For example, if Y, U, V, 4:4:4 is specified, then data is left justified out of the pipeline with the 4 LSBs padded with 0s. Also, when Y0 and Y1 are specified in the same input frame, Y0 is the first luminance component in time.

Table 3.3 Supported Pixel Word Input Formats

Pixel Word	YUV 10 bit	YUV 16 bit	RGB 16 bit	RGB 24 bit	RGB 24 bit
VSD[31:0]	Non-tagged	Tagged	Non-tagged	Tagged	Non-tagged
VSD[31]	Y1:7	Y1:7	R1:7	YAO:1	X
VSD[30]	Y1:6	Y1:6	R1:6	R1:7	X
VSD[29]	Y1:5	Y1:5	R1:5	R1:6	X
VSD[28]	Y1:4	Y1:4	R1:4	R1:5	X
VSD[27]	Y1:3	Y1:3	R1:3	R1:4	X
VSD[26]	Y1:2	Y1:2	G1:7	R1:3	X
VSD[25]	Y1:1	Y1:1	G1:6	G1:7	X
VSD[24]	Y1:0	Y1:0	G1:5	G1:6	X
VSD[23]	Y0:7	Y0:7	G1:4	G1:5	R0:7
VSD[22]	Y0:6	Y0:6	G1:3	G1:4	R0:6
VSD[21]	Y0:5	Y0:5	G1:2	G1:3	R0:5
VSD[20]	Y0:4	Y0:4	B1:7	B1:6	R0:4
VSD[19]	Y0:3	Y0:3	B1:5	B1:6	R0:3



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Table 3.3 Supported Pixel Word Input Formats

Pixel Word	YUV 18 bit	YUV 18 bit	RGB 18 bit	RGB 24 bit	RGB 24 bit
VSDP1.0	Non-tagged	Tagged	Non-tagged	Tagged	Tagged
VSDP1.0	Y0:2	Y0:2	B1:5	B0:2	R0:2
VSDP1.1	Y0:1	Y0:1	B1:4	R0:1	R0:1
VSDP1.2	Y0:0	Y0:0	B1:3	R0:0	R0:0
VSDP1.3	Y0:7	Y0:7	Y0:7	Y0:7	Y0:7
VSDP1.4	Y0:6	Y0:6	Y0:6	Y0:6	Y0:6
VSDP1.5	Y0:5	Y0:5	Y0:5	Y0:5	Y0:5
VSDP1.6	Y0:4	Y0:4	Y0:4	Y0:4	Y0:4
VSDP1.7	Y0:3	Y0:3	Y0:3	Y0:3	Y0:3
VSDP1.8	Y0:2	Y0:2	Y0:2	Y0:2	Y0:2
VSDP1.9	Y0:1	Y0:1	Y0:1	Y0:1	Y0:1
VSDP1.10	Y0:0	Y0:0	Y0:0	Y0:0	Y0:0
VSDP1.11	Y0:7	Y0:7	Y0:7	Y0:7	Y0:7
VSDP1.12	Y0:6	Y0:6	Y0:6	Y0:6	Y0:6
VSDP1.13	Y0:5	Y0:5	Y0:5	Y0:5	Y0:5
VSDP1.14	Y0:4	Y0:4	Y0:4	Y0:4	Y0:4
VSDP1.15	Y0:3	Y0:3	Y0:3	Y0:3	Y0:3
VSDP1.16	Y0:2	Y0:2	Y0:2	Y0:2	Y0:2
VSDP1.17	Y0:1	Y0:1	Y0:1	Y0:1	Y0:1
VSDP1.18	Y0:0	Y0:0	Y0:0	Y0:0	Y0:0
VSDP1.19	Y0:7	Y0:7	Y0:7	Y0:7	Y0:7
VSDP1.20	Y0:6	Y0:6	Y0:6	Y0:6	Y0:6
VSDP1.21	Y0:5	Y0:5	Y0:5	Y0:5	Y0:5
VSDP1.22	Y0:4	Y0:4	Y0:4	Y0:4	Y0:4
VSDP1.23	Y0:3	Y0:3	Y0:3	Y0:3	Y0:3
VSDP1.24	Y0:2	Y0:2	Y0:2	Y0:2	Y0:2
VSDP1.25	Y0:1	Y0:1	Y0:1	Y0:1	Y0:1
VSDP1.26	Y0:0	Y0:0	Y0:0	Y0:0	Y0:0

3.2.2.1 RGB VIDEO INPUT DATA
For RGB video input data, the Format Aligner may be programmed to accept either 5.4, 5.5, 5.6, 5.7, 5.8, or 5.9 TAG formats, where n indicates the bits allocated to the red, green, and blue planes respectively, or pseudocolor, where the most significant input byte is passed to the red, green and blue outputs. Unused bit locations should be grounded prior to FIFO input. For RGB data, the input simply passes to the output in proper bit alignment.

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3.2.2.2 YUV 4:2:2 VIDEO INPUT DATA

For 4:2:2 YUV video input data, the Format Aligner can be programmed to accept either 2 pixels of data in CCR1801 format. The Format Aligner video input format are shown on the previous page. An optional input TAG may be used in place of the LBS of the chrominance values. Note that the chrominance values align with the odd luminance values. For 4:2:2 YUV data, the Format Aligner simply passes input data, as shown in Table 3.4 on page 38, to the Chrominance Interpolator.

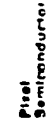
Table 3.4. YUV 4:2:2 Format

Y Frame	1	2	3	4	5	6	7	8
Y0	Y07	Y07	Y07	Y07	Y07	Y07	Y07	Y07
Y1	Y08	Y08	Y08	Y08	Y08	Y08	Y08	Y08
Y2	Y09	Y09	Y09	Y09	Y09	Y09	Y09	Y09
Y3	Y10	Y10	Y10	Y10	Y10	Y10	Y10	Y10
Y4	Y11	Y11	Y11	Y11	Y11	Y11	Y11	Y11
Y5	Y12	Y12	Y12	Y12	Y12	Y12	Y12	Y12
Y6	Y13	Y13	Y13	Y13	Y13	Y13	Y13	Y13
Y7	Y14	Y14	Y14	Y14	Y14	Y14	Y14	Y14
Y8	Y15	Y15	Y15	Y15	Y15	Y15	Y15	Y15
Y9	Y16	Y16	Y16	Y16	Y16	Y16	Y16	Y16
Y10	Y17	Y17	Y17	Y17	Y17	Y17	Y17	Y17

Chrominance Values

UV Frame	1	2	3	4
UV0	U07	U07	U07	U07
UV1	U08	U08	U08	U08
UV2	U09	U09	U09	U09
UV3	U10	U10	U10	U10
UV4	U11	U11	U11	U11
UV5	U12	U12	U12	U12
UV6	U13	U13	U13	U13
UV7	U14	U14	U14	U14
UV8	U15	U15	U15	U15
UV9	U16	U16	U16	U16
UV10	U17	U17	U17	U17

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The Chrominance Interpolator increases the sampling rate of the color difference signals when they are input at less than a 4:4:4 rate and acts as a data source for the Color Space Matrix. The Chrominance Interpolator always operates in the same mode as the format being input.

the Chrominance interpolator contains two identical circuits -- one for the U component and one for the V component. The output of the Time Demultiplexer feeds the Chrominance Interpolator logic, setting the timing U and V values to zero on display window boundary conditions.

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the Joann Corning circuit accepts input from the Color Space Monitor and outputs to the Gamma Corrector. A 4 bit room code accompanies each pixel to specify the output sequence in the CIP2000 when used with CIP2000.

The Gamma Corrector accepts input from the Color Space Matrix, and outputs to the mixing circuitry to design with: background graphics cursor, and background border. The Gamma Corrector can be programmed with a custom correction table, or to remove the gamma coding that is normally present in a TVU signal.

The Gemini Connect comprises three 256-bit memories, one for each color channel. The transfer function on each is user definable and programmable. A sample transfer function is supplied below. In this, the output of each channel is its input raised to the 2.2 power (transfer values interpreted as fractions ranging from 0 to 3535756). The transfer function is shown in Table 3.5 on page 40.

The Gamma Corrector is an optional feature and can be bypassed by the user.

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what is gamma correction

Table 3-5. Sample Gamma Removal Transfer Function

[illegible]



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3.3 Graphics Frame Buffer Interface And Processing

The CL-PX2080 accepts data from the graphics display source through either of two paths: an 8-bit VGA data path (VGA[14:0]) or a 32-bit VRAM serial data path (GSD[31:0]). One data path is selected at a time. The GFS pin and bit 5 in the CSC register determine which input is selected. These two paths are provided to allow non-generation PC graphics subsystems based on the CL-PX2080 to maintain compatibility with the large base of VGA systems while achieving higher performance and resolution in the VRAM serial data path.

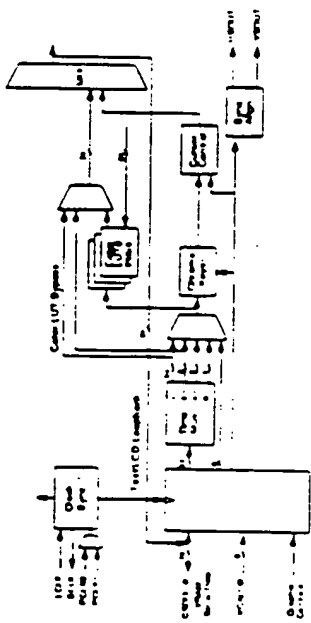


Figure 3.9 CL-PX2080 Graphics Datapath

3.3.1 VRAM Support

The graphics serial bus interface has a 32-bit data bus. The data on this bus is multiplexed under control of bits 2, 3, and 8 in the Graphics Format Control Register (GFC). Data on this bus is latched internally on the rising edge of LCLK. LCLK must be supplied by the graphics controller and should be derived from SCLK. SCLK is derived from PCLK, according to the state of bit 2 of the GFC. The maximum transfer rate on this bus is 40 MHz (32-bit words per second).

3.3.2 VGA Support

The VGA data path is an 8-bit input bus multiplexed with the VRAM serial data path under control of bit 8 of the Graphics Setup Control Register (GSC). The maximum transfer rate is 85 MHz (65 Mbytes per second). After the CL-PX2080 scales the video image, the resulting pixel data is stored in the FIFO. An external memory controller then transfers pixels from the FIFO to the display buffer memory, using addresses generated by an external pixel address calculator. The CL-PX2080 provides control signal outputs that simplify these operations.

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3.3.3 VRAM Operation

3.3.3.1 Graphics Data - GSD[31:0]

The VRAM data dock (SCLK) is generated by the CL-PX2080. In 1:1 VGA mode SCLK = LCLK. Table 3.7 describes the relationship of SCLK and LCLK in various pixel modes.

Table 3.4 SCLK and LCLK Relationships

Multiplex Rate	SCLK / LCLK Relationship
0:1	SCLK = LCLK = PCLKx8
4:1	SCLK = LCLK = PCLKx4
2:1	SCLK = LCLK = PCLKx2
1:1	SCLK = LCLK = PCLK

GSD[31:0] is the input pixel data, 8 bits per pixel (4:1 MU) and 4 bits per pixel (8:1 MU) for four and eight horizontally consecutive output pixels. GSD[31:0] is always latched on the rising edge of LCLK. The pixel dock is specified to be either PCLK or PCLK1 by bit 4 of the CSC register.

3.3.3.2 GSD[31:0] Mapping to Pixel Port Interface

Regardless of mode, the least significant word, byte, or nibble is the first to be displayed in time. For example, when in 4:1 mode, there are four 8-bit pixel ports, encoded within GSD[31:0]. Port GSD[7:0] corresponds to the first pixel of the first line of the display. This is the first pixel led to the output, followed by GSD[15:8], then GSD[23:16], and finally GSD[31:24], repeating the pattern from L50 to MSB until the first scan line is completely displayed.

3.3.3.3 Odd/Even Field Definition

The output data sequence depends on bit 3, DM of the CSC register and the ODD/EVEN input. For graphics data processing, the CL-PX2080 treats interlaced graphics data in the same manner as non-interlaced data, merely transferring it for output processing. Interlaced data alignment is performed and controlled outside the CL-PX2080. Cursor Pattern Ram Data, however, is managed by the CL-PX2080 in interlaced mode.

In interlaced mode, scan line 1 is always displayed first and is considered the first line of the EVEN field. In non-interlaced mode, scan line 2 immediately follows scan line 1. In interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the ODD/EVEN pin has toggled.

Only the ODD line or only the EVEN line will be displayed. If ODD/EVEN does not change Figure 3.10 shows the interlaced and non-interlaced display scan. Non-interlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.



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3.3.2 True Color Operation

For 16-bit color, the CL-PX2000 registers the color palette by pass feature. When by pass is selected, the pixel data are sent directly to the proper DACs of the respective DACs. By passing the palette and the pixel data, the color palette is not selected. The pixel data index the color palette in the palette, and the color palette information is passed to the respective DACs. For 16-bit color, the CL-PX2000 registers the color palette by pass feature.

For 32-bit color mapping, each independent color component of pixel data is mapped to the most significant bit of the respective palette address. The least significant bits are set to zero for contiguous palette mapping. Each independent color component of the pixel data is mapped to the least significant bit of the respective palette address. The most significant bits are set to zero for other sparse or contiguous mapping. The selected color palette values are sent to the DACs.

When 5.5 or 5.6 color format is selected, the display may contain 32 K or 64 K simultaneous colors respectively. The DACs can be configured for 8 or 16-bit resolution in this mode.

Table 3.6 Color Mapping to QSD[31:0] Bus

Format	R6	R5	R4	R3	R2	R1	R0	Q3	Q2	Q1	Q0	B3	B2	B1	B0
--------	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

5.5 Mode

Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

5.6 Mode

Format	R6	R5	R4	R3	R2	R1	R0	Q3	Q2	Q1	Q0	B3	B2	B1	B0
--------	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

5.5 Mode

Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Table 3.8 Operating Mode

VOA	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	1220	1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The pattern for the cursor is provided by the cursor RAM, which may be accessed by the BIR at any time. Cursor positioning is performed in the frame position registers (BIR-CY, BIR-CY1) Figure 3-12 demonstrates usage.

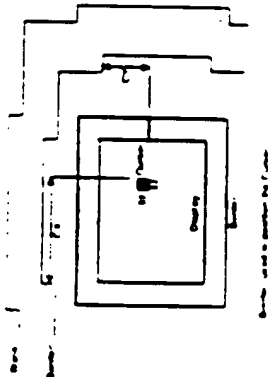


Figure 3-12 Cursor Operation

A value of 0 is written to the cursor position registers to erase the cursor completely off screen, outside the viewing area. A cursor position value of 1 places the cursor at the top right pixel of the cursor on the upper left hand corner of the screen. Only one cursor pattern per frame is displayed, regardless of updates to the cursor position registers. The single restriction on position register updates is that all position registers must be written when the cursor for given is updated.

The internal position register is updated when the Y upper byte (CY1) is written to ensure this operation. The cursor pattern is displayed at the last cursor location written prior to frame start. The reference point of the cursor, row 0 column 0, is the lower right corner of the cursor relative to BORDER1.

The position of the cursor is not dependent upon BORDER1. The cursor X position is relative to the first rising edge of CLK when BORDER1 is sampled at a logical one. The cursor Y position is relative to the first rising edge of CLK when BORDER1 is sampled at logical one after vertical blanking period has been determined.

The cursor pattern can be displayed in a interleaved system with 3, 1M of the CSC register, is a logical one. The first cursor line displayed (ROW 31 of cursor pattern RAM) depends on the state of the OCF pin and the position value in CY1, CYL. If the Y position is an even number, the data in row 31 is displayed during the even field, starting at position (CX 31, CY 31), where CX is the concatenated position determined by CXL, CYL (and similarly with Y). Each subsequent scan line displayed in the even field corresponds to every alternate active cursor line after row 31 in the cursor RAM array. During odd fields, the even rows from the cursor pattern RAM are displayed starting with row 30 at position CX 31, CY 30. Each subsequent scan line displayed in the odd field corresponds to every alternate active cursor line after row 30 in the cursor RAM array.

Similarly, if the Y position value was an odd number in the first line displayed, then Row 31 and subsequent odd rows would be displayed during an odd field. Row 30 data and subsequent even rows would be displayed during the even field.

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3.3.6 Internal Memory Access

Table 3-11. Memory Access Addressing and Indexing

Memory Access	Address BIR/PC Addr	Type R/W	Addressed by Register BIR/PC Addr	Address Range	Mod 3 Cursor Bit 1,5
Color Pattern RAM (off)	BIR-X, 007CC	W	LAW, BIR-X, 007CC	000 00FF	00
Color Pattern RAM (green)	BIR-X, 007CC	W	LAW, BIR-X, 007CC	000 00FF	01
Color Pattern RAM (blue)	BIR-X, 007CC	W	LAW, BIR-X, 007CC	000 00FF	10
Color Pattern RAM (off)	BIR-X, 007CC	R	LAR, BIR-X, 007CC	000 00FF	00
Color Pattern RAM (green)	BIR-X, 007CC	R	LAR, BIR-X, 007CC	000 00FF	01
Color Pattern RAM (blue)	BIR-X, 007CC	R	LAR, BIR-X, 007CC	000 00FF	10
Cursor Pattern RAM (off)	BIR-0, 027CC	W	VOW, BIR-0, 027CC	000 00FF	00
Cursor Pattern RAM (green)	BIR-0, 027CC	W	VOW, BIR-0, 027CC	000 00FF	01
Cursor Pattern RAM (blue)	BIR-0, 027CC	W	VOW, BIR-0, 027CC	000 00FF	10
Cursor Pattern RAM (off)	BIR-0, 027CC	R	VOR, BIR-0, 027CC	000 00FF	00
Cursor Pattern RAM (green)	BIR-0, 027CC	R	VOR, BIR-0, 027CC	000 00FF	01
Cursor Pattern RAM (blue)	BIR-0, 027CC	R	VOR, BIR-0, 027CC	000 00FF	10
Cursor Pattern Ram - Bit 0	BIR-2, 027CC	W	LAW, BIR-X, 007CC	000 00FF	NA
Cursor Pattern Ram - Bit 1	BIR-2, 027CC	W	LAW, BIR-X, 007CC	000 00FF	NA
Cursor Pattern Ram - Bit 0	BIR-2, 027CC	R	LAR, BIR-X, 007CC	000 00FF	NA
Cursor Color 1	BIR-1, 027CC	W	CAW, BIR-2, 027CC	000 00FF	00 10
Cursor Color 2	BIR-1, 027CC	W	CAW, BIR-2, 027CC	000 00FF	01 10
Cursor Color 3	BIR-1, 027CC	W	CAW, BIR-2, 027CC	000 00FF	10 10
Cursor Color 1	BIR-1, 027CC	R	CAR, BIR-2, 027CC	000 00FF	00 10
Cursor Color 2	BIR-1, 027CC	R	CAR, BIR-2, 027CC	000 00FF	01 10
Cursor Color 3	BIR-1, 027CC	R	CAR, BIR-2, 027CC	000 00FF	10 10

3.3.6.1 Color RAM Data Access

Color pattern, gamma pattern, cursor and cursor border colors are specified in terms of 24-bit RGB data, one byte per color. The host processor accesses a color memory location by first writing the index address, then performing three successive writes or reads to the data register. Upon completion of the third access, the index register points to the next location.

For example, to update the color pattern data, the processor writes the CL-P12000 address register (RAM write mode) with the address of the color pattern RAM location to be modified. The processor performs three successive write cycles (8 bits each of red, green, and blue). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the processor can modify by simply writing another sequence of red, green, and blue data. To write to a block of color values in consecutive locations, write the start address and perform continuous R, O, B write cycles until the entire block has been written. Cursor and other color information is handled the same way. Refer to appropriate Bus Interface Unit configuration for read/write timing.



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3.3.6.7 VGA Compatible Access Modes

The CL-PX2080 has the flexibility to operate in a system with a separate VGA controller/DAC or to operate in the same display output. Many currently used VGA-DAC ICs internally decode the ISA standard address for the palette RAM. The CL-PX2080 is capable of independently replacing an existing DAC, operating in parallel, or operating as a separate subsystem at a unique address. These access modes are available to maintain compatibility with software designed for VGA registers.

Mode 0 is for a system with a separate pre-existing VGA controller and palette DAC. Graphic data from the auxiliary or "feature" connector of the existing controller board enters the VGA graphics port of the CL-PX2080 where it is mixed with video data from an external source. As shown in Figure 3-13, a single

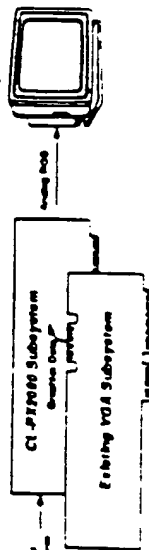


Figure 3-13: Mode 0 System Configuration

external monitor is connected to the analog RGB output of the CL-PX2080. In order to preserve the same functionality with an VGA software driver, the CL-PX2080 must respond to the standard VGA palette addresses, but not respond to reads showing the existing VGA controller board to respond. The CL-PX2080 palette RAM shadows the VGA controller RAM on writes only. Mode 0 is also useful in designs configured like that shown in Figure 3-14, when the CL-PX2080 is used with a self-decoding VGA controller.

Mode 1 is designed for a system which has a VGA controller/palette DAC and a CL-PX2080 in the same subsystem. Graphic data from the auxiliary or "feature" connector of the existing controller board enters the VGA graphics port of the CL-PX2080, where it is mixed with video data from an external source, as

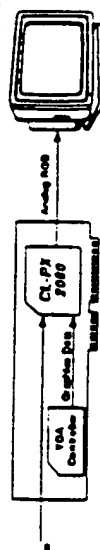


Figure 3-14: Mode 1 System Configuration

shown in Figure 3-13. The difference between modes 0 and 1 is that mode 1 responds to reads at the

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palette RAM address. This system is compatible with existing software that manipulates the VGA palette RAM.

Mode 2 is designed for a system containing a VGA controller (with palette DAC) and a CL-PX2080 subsystem, each driving separate RGB monitors, as shown in Figure 3-15. In this scenario the VGA sub-

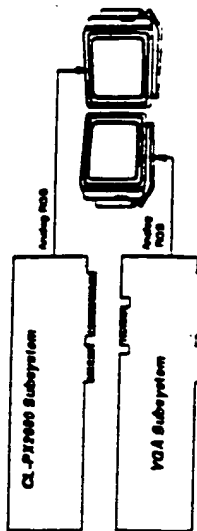


Figure 3-15: Mode 2 System Configuration

system occupies the standard VGA palette RAM addresses and the CL-PX2080 registers respond to a completely separate set of addresses.

Modes are selected by the E1, RE and R0 bits in the BIR register, described in Section 4.1.1 on page 87.

3.3.6.8 Additional Information

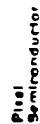
When accessing the color palette RAM, the address register reads to 00h following a blue read or write to RAM location FFh.

The processor interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between processor accesses. To reduce noticeable sparking on the CRT screen during processor access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and Look-Up Table RAMs occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (bit 1, bit 0) that count module free. They are reset to zero when the processor writes to the address register, and are not reset to zero when the processor reads the address register. The processor does not have access to these bits. The processor can read the address register at any time without modifying its contents or the existing read/write mode.

3.3.6.9 Accessing the Cursor RAM Array

The 32x32 cursor RAM is accessed in a planar format where plane 1 is bit 1 of the cursor data and plane 0 is bit 0 in the planar format, only 7 address bits are used. The eighth bit is to determine which plane (0



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Figure 3.10 Career RAM Function Diagram

whether each address in the plane, hence, the addresses themselves. The processor uses LAW or LAR (per instruction) to read the address counters to access the cursor RAM array (see Fig. 7). Note that LAW (LAW is the same binary counter used for RGB auto incrementing access to the color RAM array) is not used in the LAW after cursor auto incrementing has been initiated (as the cursor auto incrementing logic will not allow a read from the cursor RAM array has been accessed again. Cursor auto incrementing then begins from the address written in the cursor RAM. A read from the LAR does not reset the cursor auto incrementing logic. The color palette RAM and the cursor RAM share the same internal address registers, and processor addresses for this and all other registers is determined by the appropriate register addresses documented in Section Registers.

Table 3.12. Cursor Memory Mapping and Relationships for Display

BN 1	BN 0	Mode 1	Mode 2	Mode 3
0	0	Date	CC 1	Date
0	1	CC 1	CC 2	Date
	0	CC 2	Date	CC 1
	1	CC 3	Not Data	CC 2

NOTE
CCn = Cursor Color Register n
Data = Color or Gamma Palette Data
N2i = Inverse of



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3.3.6.2. 0.8N / 0.8N Operation

Bit 1, 024/118 of the ABC register, is used to specify whether the processor is reading and writing 8 bits or a byte of color information each cycle.

For 8 bit operation, D0 is the LSB and D7 is the MSB of color data.

For 0 or 8 bit operation, color data is contained on the lower 8 bits of the data bus, with D0 being the LSB and D3 the MSB of the color data. When writing color data, D0 and D7 are ignored. During color read cycles, D0 and D7 are logical zero. Accessing the cursor RAM array does not depend on the resolution of the DACs.

Note that in the 8 bit mode, the CLPX2000's full-scale output current will be less than when it is in the 3 bit mode, since the two LSBs of each 8 bit DAC are always a logical zero in the 8 bit mode.

0.3.7 Mapping to Output DAC

The Output DAC contains three 85 MHz 8 bit digital to analog converters. The table below shows how the graphic data path is controlled as the input of the DAC by BORDER, BLANK, and GPS.

Table 3.13.

	BLANK*	BORDER*	OPS
0	X	X	Video blanking
1	0	X	Border color
2	1	0	VGA or cursor color
3	1	1	OSO or cursor color

The DIP5 pin is an input used to select between the VGA and BNC graphics ports for graphics data input. "BLANK" and "SOURCE P" both prevent Graphics and Video data from being presented to the DAC. If the DIP5 pin is not used, it should be tied to the appropriate logical value for the graphics port selected.

1.9.7.1 Graphics Overlay Control

The graphics overlay controls consist of a 32-bit color key, a 32-bit color key mask, an 8-bit overlay op code, and an 8-bit multiplier.

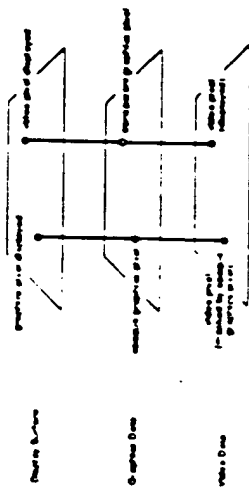
to understand how the graphics overlay controls work, imagine the CL P12000 as managing two images, one in front of the other. The two image planes are the video and graphics images, with the video image behind the graphics image. Every graphics pixel is either transparent or opaque. If the graphics pixel is opaque, the graphics color information for that pixel is displayed on the screen. If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics plane are transparent. The determination is made by a combination of two overlay control features: a TAG bit component in the video pixel data, and the graphics COLOR key switch. The graphics COLOR key switch is generated by ANDING the graphics pixel data with the GMM register, and then comparing the results against the GCK register. The tag bit is



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generated to write the CL-PX2080. The resulting signals are the select lines to the multiplexer, while the Graphics Overlay OpCodes (GOC) register is the input to the multiplexer.



3.3.2.2 Graphics Overlay OpCodes Register (GOC)

The Graphics Overlay OpCodes (GOC) is an 8-bit value used as input to an 8:1 multiplexer. The select signals to the multiplexer (the TAG bit and the graphics COLOR key match) determine which of the eight bits will become the transparent control for each pixel. The TAG bit in the GOC register is the graphics pixel become transparent, enabling the video pixel for the display. The GOC register is initialized to 0x00 during reset, selecting the graphics path and ignoring the video input stream.

3.3.3 CLK Synchronizer and SYNC Alignment

The clock generator creates all device clocks. The rising edge of LCLK latches OSD[31:0] or VOA[7:0] and BLANK, HSN, VSN, QPS and BORDER. The information latched by this signal is synchronized internally with SCLK. To avoid metastability, LCLK must maintain setup and hold requirements to SCLK. Data is synchronized with the selected pixel clock (PCLK0 or PCLK1) after being internally latched with SCLK. When the input data multiplexing rate is 8:1, 4:1, 2:1 or 1:1, LCLK must be the pixel clock divided by 8, 4, 2 or 1 respectively.

The SYNC alignment circuitry generates external HSOUT and VSOUT signals required for the monitor. The output is delayed to match the internal PCLKn delay of the RGB outputs. A SYNC Alignment Register is provided to program polarities of HSN, HSOUT, VSN, VSOUT. This register also generates a programmable PCLKn delay of RGB relative to the matched HSOUT and VSOUT, described above. This delay is programmable in both directions.

3.3.4 Power-Down Mode

The CL-PX2080 incorporates a power-down mode, controlled by bit 8 and 0 of the ASC register. While bit 8 (CKOFF) and bit 0 (DAOFF) are logical zeros, the CL-PX2080 functions normally. While bit 8 (CKOFF) is a logical one, all clock inputs, PCLKn, VCLK and LCLK, are disabled. While bit 0 (DAOFF) is a logical one, the DACs and power to the RAM are turned off.

Note that the RAM still retains the data. Also, the RAM can be read or written to by the processor as long as the pixel clock is running. The RAM automatically powers up during processor read/write cycles, and shuts down when the processor access is completed. The DACs output no current, and the three command registers can still be written to or read by the processor.



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4. REGISTERS

Internal registers control the operations of the CL-PX2000. These registers are organized in mapping order in Table 4.1 on page 57. Table 5.2 on page 72 summarizes the CL-PX2000 registers, and organizes them according to the following functions:

- Indexing
- CLUT Access
- Cursor Access
- Video, Graphics, and Cursor Control
- Video Gamma Correction Palette Access
- Graphics Overlay Control
- Cursor Positioning
- Digital to Analog Conversion and Control

NOTE: Data values reserved register locations are not guaranteed on readback. Reserved bits in unused register locations are read back as 0.

Table 4.1. CL-PX2000 Control Registers (Organized by Mapping)

NOTE: Register bit fields addressing in microprocessor mode (IO address and Bit) (Base Index Register) apply to ISA and MCA modes.

Register	RS[4:3]	Prt. I/O Addr	See Addr	BitR	Definition	Ref. Section
BIR	N/A	0x27CE	0x029E	N/A	Block Index Register	4.1.1, p. 58
AW	0x00	0x02C9	N/A	N/A	CLUT Write Address	4.2.1, p. 60
CD	0x01	0x02C9	N/A	N/A	CLUT Color Data	4.2.2, p. 61
PM	0x02	0x02C9	N/A	N/A	CLUT Pixel Mask	4.2.3, p. 62
AR	0x03	0x02C7	N/A	N/A	CLUT Read Address	4.2.4, p. 63
AW	0x04	0x27CC	0x029C	1	Cursor Address Write 2	4.3.1, p. 64
CD	0x05	0x27CD	0x029D	1	Cursor Color Data Register	4.3.2, p. 64
SC	0x06	0x27CA	0x029A	1	Analog Setup Control	4.8.1, p. 79
AR	0x07	0x27CB	0x029B	1	Cursor Address Read	4.3.3, p. 65
FC	0x08	0x27CC	0x029C	2	Graphics Format Control	4.4.2, p. 67
BC	0x09	0x27CD	0x029D	2	Cursor Setup Control	4.4.3, p. 68
SR	0x0A	0x27CA	0x029A	2	Graphics Status Register	4.4.1, p. 66
PR	0x0B	0x27CB	0x029B	2	Cursor Pattern RAM	4.3.4, p. 65
XL	0x0C	0x27CC	0x029C	3	Cursor X Position, Low Byte	4.7.1, p. 75
XR	0x0D	0x27CD	0x029D	3	Cursor X Position, High Byte	4.7.1, p. 75

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Table 4-1: CL-PX2000 Control Registers (Organized by Mapping)

NOTE: All registers are read-only. The CLUT access registers (CLUT0-CLUT7) are read-only and are not mapped to the CLUT access registers.

Register	Register Name	Bit IO Addr	Sec Addr	BIR	Definition	Ref. Section
CLUT0	CLUT0	0x0000	0x0000	3	Cursor 1 Position, Low Byte	4.1.2 p. 16
CLUT1	CLUT1	0x0001	0x0001	3	Cursor 1 Position, High Byte	4.1.2 p. 16
CLUT2	CLUT2	0x0002	0x0002	3	Cursor 2 Position, Low Byte	4.1.2 p. 16
CLUT3	CLUT3	0x0003	0x0003	3	Cursor 2 Position, High Byte	4.1.2 p. 16
CLUT4	CLUT4	0x0004	0x0004	3	Cursor 3 Position, Low Byte	4.1.2 p. 16
CLUT5	CLUT5	0x0005	0x0005	3	Cursor 3 Position, High Byte	4.1.2 p. 16
CLUT6	CLUT6	0x0006	0x0006	3	Cursor 4 Position, Low Byte	4.1.2 p. 16
CLUT7	CLUT7	0x0007	0x0007	3	Cursor 4 Position, High Byte	4.1.2 p. 16
CLUT8	CLUT8	0x0008	0x0008	3	Cursor 5 Position, Low Byte	4.1.2 p. 16
CLUT9	CLUT9	0x0009	0x0009	3	Cursor 5 Position, High Byte	4.1.2 p. 16
CLUT10	CLUT10	0x000A	0x000A	3	Cursor 6 Position, Low Byte	4.1.2 p. 16
CLUT11	CLUT11	0x000B	0x000B	3	Cursor 6 Position, High Byte	4.1.2 p. 16
CLUT12	CLUT12	0x000C	0x000C	3	Cursor 7 Position, Low Byte	4.1.2 p. 16
CLUT13	CLUT13	0x000D	0x000D	3	Cursor 7 Position, High Byte	4.1.2 p. 16
CLUT14	CLUT14	0x000E	0x000E	3	Cursor 8 Position, Low Byte	4.1.2 p. 16
CLUT15	CLUT15	0x000F	0x000F	3	Cursor 8 Position, High Byte	4.1.2 p. 16
CLUT16	CLUT16	0x0010	0x0010	3	Cursor 9 Position, Low Byte	4.1.2 p. 16
CLUT17	CLUT17	0x0011	0x0011	3	Cursor 9 Position, High Byte	4.1.2 p. 16
CLUT18	CLUT18	0x0012	0x0012	3	Cursor 10 Position, Low Byte	4.1.2 p. 16
CLUT19	CLUT19	0x0013	0x0013	3	Cursor 10 Position, High Byte	4.1.2 p. 16
CLUT20	CLUT20	0x0014	0x0014	3	Cursor 11 Position, Low Byte	4.1.2 p. 16
CLUT21	CLUT21	0x0015	0x0015	3	Cursor 11 Position, High Byte	4.1.2 p. 16
CLUT22	CLUT22	0x0016	0x0016	3	Cursor 12 Position, Low Byte	4.1.2 p. 16
CLUT23	CLUT23	0x0017	0x0017	3	Cursor 12 Position, High Byte	4.1.2 p. 16
CLUT24	CLUT24	0x0018	0x0018	3	Cursor 13 Position, Low Byte	4.1.2 p. 16
CLUT25	CLUT25	0x0019	0x0019	3	Cursor 13 Position, High Byte	4.1.2 p. 16
CLUT26	CLUT26	0x001A	0x001A	3	Cursor 14 Position, Low Byte	4.1.2 p. 16
CLUT27	CLUT27	0x001B	0x001B	3	Cursor 14 Position, High Byte	4.1.2 p. 16
CLUT28	CLUT28	0x001C	0x001C	3	Cursor 15 Position, Low Byte	4.1.2 p. 16
CLUT29	CLUT29	0x001D	0x001D	3	Cursor 15 Position, High Byte	4.1.2 p. 16
CLUT30	CLUT30	0x001E	0x001E	3	Cursor 16 Position, Low Byte	4.1.2 p. 16
CLUT31	CLUT31	0x001F	0x001F	3	Cursor 16 Position, High Byte	4.1.2 p. 16
CLUT32	CLUT32	0x0020	0x0020	3	Cursor 17 Position, Low Byte	4.1.2 p. 16
CLUT33	CLUT33	0x0021	0x0021	3	Cursor 17 Position, High Byte	4.1.2 p. 16
CLUT34	CLUT34	0x0022	0x0022	3	Cursor 18 Position, Low Byte	4.1.2 p. 16
CLUT35	CLUT35	0x0023	0x0023	3	Cursor 18 Position, High Byte	4.1.2 p. 16
CLUT36	CLUT36	0x0024	0x0024	3	Cursor 19 Position, Low Byte	4.1.2 p. 16
CLUT37	CLUT37	0x0025	0x0025	3	Cursor 19 Position, High Byte	4.1.2 p. 16
CLUT38	CLUT38	0x0026	0x0026	3	Cursor 20 Position, Low Byte	4.1.2 p. 16
CLUT39	CLUT39	0x0027	0x0027	3	Cursor 20 Position, High Byte	4.1.2 p. 16
CLUT40	CLUT40	0x0028	0x0028	3	Cursor 21 Position, Low Byte	4.1.2 p. 16
CLUT41	CLUT41	0x0029	0x0029	3	Cursor 21 Position, High Byte	4.1.2 p. 16
CLUT42	CLUT42	0x002A	0x002A	3	Cursor 22 Position, Low Byte	4.1.2 p. 16
CLUT43	CLUT43	0x002B	0x002B	3	Cursor 22 Position, High Byte	4.1.2 p. 16
CLUT44	CLUT44	0x002C	0x002C	3	Cursor 23 Position, Low Byte	4.1.2 p. 16
CLUT45	CLUT45	0x002D	0x002D	3	Cursor 23 Position, High Byte	4.1.2 p. 16
CLUT46	CLUT46	0x002E	0x002E	3	Cursor 24 Position, Low Byte	4.1.2 p. 16
CLUT47	CLUT47	0x002F	0x002F	3	Cursor 24 Position, High Byte	4.1.2 p. 16
CLUT48	CLUT48	0x0030	0x0030	3	Cursor 25 Position, Low Byte	4.1.2 p. 16
CLUT49	CLUT49	0x0031	0x0031	3	Cursor 25 Position, High Byte	4.1.2 p. 16
CLUT50	CLUT50	0x0032	0x0032	3	Cursor 26 Position, Low Byte	4.1.2 p. 16
CLUT51	CLUT51	0x0033	0x0033	3	Cursor 26 Position, High Byte	4.1.2 p. 16
CLUT52	CLUT52	0x0034	0x0034	3	Cursor 27 Position, Low Byte	4.1.2 p. 16
CLUT53	CLUT53	0x0035	0x0035	3	Cursor 27 Position, High Byte	4.1.2 p. 16
CLUT54	CLUT54	0x0036	0x0036	3	Cursor 28 Position, Low Byte	4.1.2 p. 16
CLUT55	CLUT55	0x0037	0x0037	3	Cursor 28 Position, High Byte	4.1.2 p. 16
CLUT56	CLUT56	0x0038	0x0038	3	Cursor 29 Position, Low Byte	4.1.2 p. 16
CLUT57	CLUT57	0x0039	0x0039	3	Cursor 29 Position, High Byte	4.1.2 p. 16
CLUT58	CLUT58	0x003A	0x003A	3	Cursor 30 Position, Low Byte	4.1.2 p. 16
CLUT59	CLUT59	0x003B	0x003B	3	Cursor 30 Position, High Byte	4.1.2 p. 16
CLUT60	CLUT60	0x003C	0x003C	3	Cursor 31 Position, Low Byte	4.1.2 p. 16
CLUT61	CLUT61	0x003D	0x003D	3	Cursor 31 Position, High Byte	4.1.2 p. 16
CLUT62	CLUT62	0x003E	0x003E	3	Cursor 32 Position, Low Byte	4.1.2 p. 16
CLUT63	CLUT63	0x003F	0x003F	3	Cursor 32 Position, High Byte	4.1.2 p. 16
CLUT64	CLUT64	0x0040	0x0040	3	Cursor 33 Position, Low Byte	4.1.2 p. 16
CLUT65	CLUT65	0x0041	0x0041	3	Cursor 33 Position, High Byte	4.1.2 p. 16
CLUT66	CLUT66	0x0042	0x0042	3	Cursor 34 Position, Low Byte	4.1.2 p. 16
CLUT67	CLUT67	0x0043	0x0043	3	Cursor 34 Position, High Byte	4.1.2 p. 16
CLUT68	CLUT68	0x0044	0x0044	3	Cursor 35 Position, Low Byte	4.1.2 p. 16
CLUT69	CLUT69	0x0045	0x0045	3	Cursor 35 Position, High Byte	4.1.2 p. 16
CLUT70	CLUT70	0x0046	0x0046	3	Cursor 36 Position, Low Byte	4.1.2 p. 16
CLUT71	CLUT71	0x0047	0x0047	3	Cursor 36 Position, High Byte	4.1.2 p. 16
CLUT72	CLUT72	0x0048	0x0048	3	Cursor 37 Position, Low Byte	4.1.2 p. 16
CLUT73	CLUT73	0x0049	0x0049	3	Cursor 37 Position, High Byte	4.1.2 p. 16
CLUT74	CLUT74	0x004A	0x004A	3	Cursor 38 Position, Low Byte	4.1.2 p. 16
CLUT75	CLUT75	0x004B	0x004B	3	Cursor 38 Position, High Byte	4.1.2 p. 16
CLUT76	CLUT76	0x004C	0x004C	3	Cursor 39 Position, Low Byte	4.1.2 p. 16
CLUT77	CLUT77	0x004D	0x004D	3	Cursor 39 Position, High Byte	4.1.2 p. 16
CLUT78	CLUT78	0x004E	0x004E	3	Cursor 40 Position, Low Byte	4.1.2 p. 16
CLUT79	CLUT79	0x004F	0x004F	3	Cursor 40 Position, High Byte	4.1.2 p. 16
CLUT80	CLUT80	0x0050	0x0050	3	Cursor 41 Position, Low Byte	4.1.2 p. 16
CLUT81	CLUT81	0x0051	0x0051	3	Cursor 41 Position, High Byte	4.1.2 p. 16
CLUT82	CLUT82	0x0052	0x0052	3	Cursor 42 Position, Low Byte	4.1.2 p. 16
CLUT83	CLUT83	0x0053	0x0053	3	Cursor 42 Position, High Byte	4.1.2 p. 16
CLUT84	CLUT84	0x0054	0x0054	3	Cursor 43 Position, Low Byte	4.1.2 p. 16
CLUT85	CLUT85	0x0055	0x0055	3	Cursor 43 Position, High Byte	4.1.2 p. 16
CLUT86	CLUT86	0x0056	0x0056	3	Cursor 44 Position, Low Byte	4.1.2 p. 16
CLUT87	CLUT87	0x0057	0x0057	3	Cursor 44 Position, High Byte	4.1.2 p. 16
CLUT88	CLUT88	0x0058	0x0058	3	Cursor 45 Position, Low Byte	4.1.2 p. 16
CLUT89	CLUT89	0x0059	0x0059	3	Cursor 45 Position, High Byte	4.1.2 p. 16
CLUT90	CLUT90	0x005A	0x005A	3	Cursor 46 Position, Low Byte	4.1.2 p. 16
CLUT91	CLUT91	0x005B	0x005B	3	Cursor 46 Position, High Byte	4.1.2 p. 16
CLUT92	CLUT92	0x005C	0x005C	3	Cursor 47 Position, Low Byte	4.1.2 p. 16
CLUT93	CLUT93	0x005D	0x005D	3	Cursor 47 Position, High Byte	4.1.2 p. 16
CLUT94	CLUT94	0x005E	0x005E	3	Cursor 48 Position, Low Byte	4.1.2 p. 16
CLUT95	CLUT95	0x005F	0x005F	3	Cursor 48 Position, High Byte	4.1.2 p. 16
CLUT96	CLUT96	0x0060	0x0060	3	Cursor 49 Position, Low Byte	4.1.2 p. 16
CLUT97	CLUT97	0x0061	0x0061	3	Cursor 49 Position, High Byte	4.1.2 p. 16
CLUT98	CLUT98	0x0062	0x0062	3	Cursor 50 Position, Low Byte	4.1.2 p. 16
CLUT99	CLUT99	0x0063	0x0063	3	Cursor 50 Position, High Byte	4.1.2 p. 16
CLUT100	CLUT100	0x0064	0x0064	3	Cursor 51 Position, Low Byte	4.1.2 p. 16
CLUT101	CLUT101	0x0065	0x0065	3	Cursor 51 Position, High Byte	4.1.2 p. 16
CLUT102	CLUT102	0x0066	0x0066	3	Cursor 52 Position, Low Byte	4.1.2 p. 16
CLUT103	CLUT103	0x0067	0x0067	3	Cursor 52 Position, High Byte	4.1.2 p. 16
CLUT104	CLUT104	0x0068	0x0068	3	Cursor 53 Position, Low Byte	4.1.2 p. 16
CLUT105	CLUT105	0x0069	0x0069	3	Cursor 53 Position, High Byte	4.1.2 p. 16
CLUT106	CLUT106	0x006A	0x006A	3	Cursor 54 Position, Low Byte	4.1.2 p. 16
CLUT107	CLUT107	0x006B	0x006B	3	Cursor 54 Position, High Byte	4.1.2 p. 16
CLUT108	CLUT108	0x006C	0x006C	3	Cursor 55 Position, Low Byte	4.1.2 p. 16
CLUT109	CLUT109	0x006D	0x006D	3	Cursor 55 Position, High Byte	4.1.2 p. 16
CLUT110	CLUT110	0x006E	0x006E	3	Cursor 56 Position, Low Byte	4.1.2 p. 16
CLUT111	CLUT111	0x006F	0x006F	3	Cursor 56 Position, High Byte	4.1.2 p. 16
CLUT112	CLUT112	0x0070	0x0070	3	Cursor 57 Position, Low Byte	4.1.2 p. 16
CLUT113	CLUT113	0x0071	0x0071	3	Cursor 57 Position, High Byte	4.1.2 p. 16
CLUT114	CLUT114	0x0072	0x0072	3	Cursor 58 Position, Low Byte	4.1.2 p. 16
CLUT115	CLUT115	0x0073	0x0073	3	Cursor 58 Position, High Byte	4.1.2 p. 16
CLUT116	CLUT116	0x0074	0x0074	3	Cursor 59 Position, Low Byte	4.1.2 p. 16
CLUT117	CLUT117	0x0075	0x0075	3	Cursor 59 Position, High Byte	4.1.2 p. 16
CLUT118	CLUT118	0x0076	0x0076	3	Cursor 60 Position, Low Byte	4.1.2 p. 16
CLUT119	CLUT119	0x0077	0x0077	3	Cursor 60 Position, High Byte	4.1.2 p. 16
CLUT120	CLUT120	0x0078	0x0078	3	Cursor 61 Position, Low Byte	4.1.2 p. 16
CLUT121	CLUT121	0x0079	0x0079	3	Cursor 61 Position, High Byte	4.1.2 p. 16
CLUT122	CLUT122	0x007A	0x007A	3	Cursor 62 Position, Low Byte	4.1.2 p. 16
CLUT123	CLUT123	0x007B	0x007B	3	Cursor 62 Position, High Byte	4.1.2 p. 16
CLUT124	CLUT124	0x007C	0x007C	3	Cursor 63 Position, Low Byte	4.1.2 p. 16
CLUT125	CLUT125	0x007D	0x007D	3	Cursor 63 Position, High Byte	4.1.2 p. 16
CLUT126	CLUT126	0x007E	0x007E	3	Cursor 64 Position, Low Byte	4.1.2 p. 16
CLUT127	CLUT127	0x007F	0x007F	3	Cursor 64 Position, High Byte	4.1.2 p. 16
CLUT128	CLUT128	0x0080	0x0080	3	Cursor 65 Position, Low Byte	4.1.2 p. 16
CLUT129	CLUT129	0x0081	0x0081	3	Cursor 65 Position, High Byte	4.1.2 p. 16
CLUT130	CLUT130	0x0082	0x0082	3	Cursor 66 Position, Low Byte	4.1.2 p. 16
CLUT131	CLUT131	0x0083	0x0083	3	Cursor 66 Position, High Byte	4.1.2 p. 16
CLUT132	CLUT132	0x0084	0x0084	3	Cursor 67 Position, Low Byte	4.1.2 p. 16
CLUT133	CLUT133	0x0085	0x0085	3	Cursor 67 Position, High Byte	4.1.2 p. 16
CLUT134	CLUT134	0x0086	0x0086	3	Cursor 68 Position, Low Byte	4.1.2 p. 16
CLUT135	CLUT135	0x0087	0x0087	3	Cursor 68 Position, High Byte	4.1.2 p. 16
CLUT136	CLUT136	0x0088	0x0088	3	Cursor 69 Position, Low Byte	4.1.2 p. 16
CLUT137	CLUT137	0x0089	0x0089	3	Cursor 69 Position, High Byte	4.1.2 p. 16
CLUT138	CLUT138	0x008A	0x008A	3	Cursor 70 Position, Low Byte	4.1.2 p. 16
CLUT139	CLUT139	0x008B	0x008B	3	Cursor 70 Position, High Byte	4.1.2 p. 16
CLUT140	CLUT140	0x008C	0x008C	3	Cursor 71 Position, Low Byte	4.1.2 p. 16
CLUT141	CLUT141	0x008D	0x008D	3	Cursor 71 Position, High Byte	4.1.2 p. 16
CLUT142	CLUT142	0x008E	0x008E	3	Cursor 72 Position, Low Byte	4.1.2 p. 16
CLUT143	CLUT143	0x008F	0x008F	3	Cursor 72 Position, High Byte	4.1.2 p. 16
CLUT144	CLUT144	0x0090	0x0090	3	Cursor 73 Position, Low Byte	4.1.2 p. 16
CLUT145	CLUT145	0x0091	0x0091	3	Cursor 73 Position, High Byte	4.1.2 p. 16
CLUT146	CLUT146	0x0092	0x0092	3	Cursor 74 Position, Low Byte	4.1.2 p. 16
CLUT147	CLUT147	0x0093	0x0093	3	Cursor 74 Position, High Byte	4.1.2 p. 16
CLUT148	CLUT148	0x0094	0x0094	3	Cursor 75 Position, Low Byte	4.1.2 p. 16
CLUT149	CLUT149	0x0095	0x0095	3	Cursor 75 Position, High Byte	

CLUT AGENT

The graphics ConLookUp table (CUT) expands a 0 and 1 to graphics pixel data in 16 or 24 bits, and the address modes are described in 3.8.2 p. 50.

021 LAW CLUT W/NO ADDRESS

NO A-10-000	ISA MCA Model	0-07100
Item Code: Regulator	ISA MCA Model	N/A
Item Address	ISA MCA Model	0-07100

1111 Wm. Address Neglect: AWW, a module 256 counsell, shows new functions -- palette rotation and cursor pattern selection

Platform Color: Red/Black

penalty color, selection mode (AW specifies the 2nd or 10th graphics palette color) to be written to register LCD on the next write operation (AW specifies the same palette color) for entries cycles N and N+1 with cycle N (AW automatically increments by one to specify the next palette color).

Figure 2 is a line graph with the X-axis labeled 'Number of days after the start of the rainy season' ranging from 0 to 100 in increments of 20. The Y-axis is labeled 'Number of days until the start of the rainy season' ranging from 0 to 100 in increments of 20. The graph displays a series of data points connected by lines, showing a fluctuating pattern. The data points are approximately as follows:

Number of days after the start of the rainy season	Number of days until the start of the rainy season
0	10
20	20
40	30
60	40
80	50
100	60
120	70
140	80
160	90
180	100
200	110
220	120
240	130
260	140
280	150
300	160
320	170
340	180
360	190
380	200
400	210
420	220
440	230
460	240
480	250
500	260
520	270
540	280
560	290
580	300
600	310
620	320
640	330
660	340
680	350
700	360
720	370
740	380
760	390
780	400
800	410
820	420
840	430
860	440
880	450
900	460
920	470
940	480
960	490
980	500
1000	510
1020	520
1040	530
1060	540
1080	550
1100	560
1120	570
1140	580
1160	590
1180	600
1200	610
1220	620
1240	630
1260	640
1280	650
1300	660
1320	670
1340	680
1360	690
1380	700
1400	710
1420	720
1440	730
1460	740
1480	750
1500	760
1520	770
1540	780
1560	790
1580	800
1600	810
1620	820
1640	830
1660	840
1680	850
1700	860
1720	870
1740	880
1760	890
1780	900
1800	910
1820	920
1840	930
1860	940
1880	950
1900	960
1920	970
1940	980
1960	990
1980	1000
2000	1010
2020	1020
2040	1030
2060	1040
2080	1050
2100	1060
2120	1070
2140	1080
2160	1090
2180	1100
2200	1110
2220	1120
2240	1130
2260	1140
2280	1150
2300	1160
2320	1170
2340	1180
2360	1190
2380	1200
2400	1210
2420	1220
2440	1230
2460	1240
2480	1250
2500	1260
2520	1270
2540	1280
2560	1290
2580	1300
2600	1310
2620	1320
2640	1330
2660	1340
2680	1350
2700	1360
2720	1370
2740	1380
2760	1390
2780	1400
2800	1410
2820	1420
2840	1430
2860	1440
2880	1450
2900	1460
2920	1470
2940	1480
2960	1490
2980	1500
3000	1510
3020	1520
3040	1530
3060	1540
3080	1550
3100	1560
3120	1570
3140	1580
3160	1590
3180	1600
3200	1610
3220	1620
3240	1630
3260	1640
3280	1650
3300	1660
3320	1670
3340	1680
3360	1690
3380	1700
3400	1710
3420	1720
3440	1730
3460	1740
3480	1750
3500	1760
3520	1770
3540	1780
3560	1790
3580	1800
3600	1810
3620	1820
3640	1830
3660	1840
3680	1850
3700	1860
3720	1870
3740	1880
3760	1890
3780	1900
3800	1910
3820	1920
3840	1930
3860	1940
3880	1950
3900	1960
3920	1970
3940	1980
3960	1990
3980	2000
4000	2010
4020	2020
4040	2030
4060	2040
4080	2050
4100	2060
4120	2070
4140	2080
4160	2090
4180	2100
4200	2110
4220	2120
4240	2130
4260	2140
4280	2150
4300	2160
4320	2170
4340	2180
4360	2190
4380	2200
4400	2210
4420	2220
4440	2230
4460	2240
4480	2250
4500	2260
4520	2270
4540	2280
4560	2290
4580	2300
4600	2310
4620	2320
4640	2330
4660	2340
4680	2350
4700	2360
4720	2370
4740	2380
4760	2390
4780	2400
4800	2410
4820	2420
4840	2430
4860	2440
4880	2450
4900	2460
4920	2470
4940	2480
4960	2490
4980	2500
5000	2510
5020	2520
5040	2530
5060	2540
5080	2550
5100	2560
5120	2570
5140	2580
5160	2590
5180	2600
5200	2610
5220	2620
5240	2630
5260	2640
5280	2650
5300	2660
5320	2670
5340	2680
5360	2690
5380	2700
5400	2710
5420	2720
5440	2730
5460	2740
5480	2750
5500	2760
5520	2770
5540	2780
5560	2790
5580	2800
5600	2810
5620	2820
5640	2830
5660	2840
5680	2850
5700	2860
5720	2870
5740	2880
5760	2890
5780	2900
5800	2910
5820	2920
5840	2930
5860	2940
5880	2950
5900	2960
5920	2970
5940	2980
5960	2990
5980	3000
6000	3010
6020	3020
6040	3030
6060	3040
6080	3050
6100	3060
6120	3070
6140	3080
6160	3090
6180	3100
6200	3110
6220	3120
6240	3130
6260	3140
6280	3150
6300	3160
6320	3170
6340	3180
6360	3190
6380	3200
6400	3210
6420	3220
6440	3230
6460	3240
6480	3250
6500	3260
6520	3270
6540	3280
6560	3290
6580	3300
6600	3310
6620	3320
6640	3330
6660	3340
6680	3350
6700	3360
6720	3370
6740	3380
6760	3390
6780	3400
6800	3410
6820	3420
6840	3430
6860	3440
6880	3450
6900	3460
6920	3470
6940	3480
6960	3490
6980	3500
7000	3510
7020	3520
7040	3530
7060	3540
7080	3550
7100	3560
7120	3570
7140	3580
7160	3590
7180	3600
7200	3610
7220	3620
7240	3630
7260	3640
7280	3650
7300	3660
7320	3670
7340	3680
7360	3690
7380	3700
7400	3710
7420	3720
7440	3730
7460	3740
7480	3750
7500	3760
7520	3770
7540	3780
7560	3790
7580	3800
7600	3810
7620	3820
7640	3830
7660	3840
7680	3850
7700	3860
7720	3870
7740	3880
7760	3890
7780	3900
7800	3910
7820	3920
7840	3930
7860	3940
7880	3950
7900	3960
7920	3970
7940	3980
7960	3990
7980	4000
8000	4010
8020	4020
8040	4030
8060	4040
8080	4050
8100	4060
8120	4070
8140	4080
8160	4090
8180	4100
8200	4110
8220	4120
8240	4130
8260	4140
8280	4150
8300	4160
8320	4170
8340	4180
8360	4190
8380	4200
8400	4210
8420	4220
8440	4230
8460	4240
8480	4250
8500	4260
8520	4270
8540	4280
8560	4290
8580	4300
8600	4310
8620	4320
8640	4330
8660	4340
8680	4350
8700	4360
8720	4370
8740	4380
8760	4390
8780	4400
8800	4410
8820	4420
8840	4430
8860	4440
8880	4450
8900	4460
8920	4470
8940	4480
8960	4490
8980	4500
9000	4510
9020	4520
9040	4530
9060	4540
9080	4550
9100	4560
9120	4570
9140	4580
9160	4590
9180	4600
9200	4610
9220	4620
9240	4630
9260	4640
9280	4650
9300	4660
9320	4670
9340	4680
9360	4690
9380	4700
9400	4710
9420	4720
9440	4730
9460	4740
9480	4750
9500	4760
9520	4770
9540	4780
9560	4790
9580	4800
9600	4810
9620	4820
9640	4830
9660	4840
9680	4850
9700	4860
9720	4870
9740	4880
9760	4890
9780	4900
9800	4910
9820	4920
9840	4930
9860	4940
9880	4950
9900	4960
9920	4970
9940	4980
9960	4990
9980	5000
10000	5010

no	Access	Reset	Description
0	RW	DA	WA Write Address to 64000 RAM

Linear Pattern Detection

cursor pattern selection mode. LAW addresses the cursor pattern RAM, which comprises two 32x32 or 48x32 bit planes, for a total of 128 bytes in each plane. LAW automatically increments when writing register CFn.

Q	WPA										Q
1	0	0	0	4	0	0	0	0	0	0	0

#	Access	Reset	Description
R/W	0	P	Plane Select: The cursor bit plane to be addressed 0 L38 plane of cursor ram 1 L39 plane of cursor ram
R/W	0h	WA	Write Address for cursor RAM: Byte address of cursor plane (8 per address) being addressed for the 128 bytes in cursor RAM. Bytes 30 are the four bytes of the top row.



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4.3.2 LCD: CLUT Color Data

I/O Address	(ISA, MCA Model)	0-03C9
Base Index Register	(ISA, MCA Model)	N/A
Direct Address	(Coprocessor Mode)	0-01

Port LCD is an 8-bit wide path to the graphics color palette — a 256x18- or 24-bit memory array LCD must be addressed three times, once for each palette color.

For read operations:

- The first read operation reads the red 0: 0: 0: 0: 0 component (as specified by register ASC, bit D21) of the palette color specified by LAR.
- The second read operation reads the green 0: 0: 0: 0: 0 component of the palette color specified by LAR.

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- The third read operation reads the blue 6- or 8-bit component of the pellets color specified by LAIN. After the blue component is read, register LAIN automatically increments to the next pellet color. When in 6-bit mode, the data shifts left two bits, and the two LSBs are padded with zeros before a tracking into the data bus.

For extra questions:

- The first write operation writes the red 8, or 8 bit component of the palette color specified by LAW.
The second write operation writes the green 8, or 8 bit component of the palette color specified by LAW.

- The third write operation writes the blue 6- or 8-bit component of the palette color specified by LAW. After the blue component is written, register LAW automatically increments to the next palette color. When in 8-bit mode, the data shifts left two bits and the two LSBs are padded with zeros before a loading into the palette.

[illegible]

Ln #	Amount	Receipt	Description
1	2	POW	Ch D Color LUT Data



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4.2.3 LPM CLUT Pixel Mask

IO Address (ISA MCA Modes) P-070 &
Base Index Register (ISA MCA Modes) N/A
Data Address (Coprocessor Mode) 0-077

The graphics pixel data used to form up color information in the palette can be masked before the lookup operation. Register P070 masks the address. The 8 or 6 bit graphics pixel is logically AND'ed with the P070 data and the result is used to address the color palette.

7	6	5	4	3	2	1	0

Bit 0 Access Reset Description

IO RW IN M CLUT Pixel Mask

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4.2.4 LAR: CLUT Read Address

IO Address (ISA MCA Modes) 0-07C7
Base Index Register (ISA MCA Modes) N/A
Data Address (Coprocessor Mode) 0-077

CLUT Read Address register LAR is a modulo 256 counter that shares two functions: palette color selection and cursor pattern selection.

Palette Color Selection

In palette color selection mode, LAR specifies the 24- or 16-bit graphics palette color to be read on the next read operation to register LCD. LAR specifies the same palette color for read cycles R.O. and B. After read cycle B, LAR automatically increments by one to specify the next palette color.

7	6	5	4	3	2	1	0

Bit 0 Access Reset Description

IO RW O NA CLUT Read Address

Cursor Pattern Selection

In cursor pattern selection mode, LAR addresses the cursor pattern RAM, which comprises two 32x32 bit or 4x32 byte planes, for a total of 128 bytes in each plane. LAR automatically increments when writing to register CTR.

7	6	5	4	3	2	1	0

Bit 0 Access Reset Description

IO RW O P Plane Specifying the cursor bit plane to be addressed

0 LSB plane of cursor RAM
1 MSB plane of cursor RAM

Bit 0 RW O NA CLUT Read Address. Byte address of cursor plane (0 plane address is the first address for the 128 bytes in cursor RAM. Bytes 30 are the four bytes of the top row.)

0 The LSB plane of cursor RAM.
1 The MSB plane of cursor RAM.

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6.3 Cursor Access

6.3.1 CAW Cursor Address Write
IO Address (ISA, MCA Modes) 0-077C
Base Index Register (ISA, MCA Modes) 1
Direct Address (Coprocessor Mode) 0-07C

Cursor Address Write register (CAW) is a module 4 counter that specifies the 24 bit cursor or border color register that is to be modified on the next operation to register CCD. CAW specifies the same cursor color register for write cycles R, G, and B. After write cycle R, CAW automatically increments by one to specify the next cursor color register.

Bit #	RWD				RA			
	7	6	5	4	3	2	1	0

Bit # Access Reset Description

7:2	RW	0	RWD	Reserved (write as zero)
1:0	RW	0	RA	Cursor Write Address

6.3.2 CCD Cursor Color Data Registers

IO Address (ISA, MCA Modes) 0-07ED
Base Index Register (ISA, MCA Modes) 1
Direct Address (Coprocessor Mode) 0-07D

See also Table 3.11 Memory Access Addressing and Indexing p. 48
Figure 3.13 Cursor RAM Function Diagram p. 49

Port CCD accesses three 24 bit cursor and border color registers

- For cursor color read operations, register CAR must point to the cursor color to be read
- For cursor color write operations, register CAW must point to the cursor color to be written

CAR and CAW point to the red component of each color only

Three IO operations — R, G, and B — must take place for each color. CAR and CAW automatically increment by one after IO operation B. The components must be read and/or written in the following order: red, green, blue

Bit #	RWD				D			
	7	6	5	4	3	2	1	0

Bit # Access Reset Description

7	RW	0	D	Color Data
---	----	---	---	------------

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4.3.3 CAR Cursor Address Read

IO Address (ISA, MCA Modes) 0-07EB
Base Index Register (ISA, MCA Modes) 1
Direct Address (Coprocessor Mode) 0-07B

Register CAR is a module 4 counter that specifies the 24 bit cursor color register to be read on the next read operation to register CCD. CAR specifies the same cursor color register for read cycles R, G, and B. After read cycle B, CAR automatically increments by one to specify the next cursor color register.

Bit #	RWD				RA			
	7	6	5	4	3	2	1	0

Bit # Access Reset Description

7:2	RW	0	RWD	Reserved (write as zero)
1:0	RW	0	RA	Cursor Read Address

4.3.4 CPR: Cursor Pattern RAM

IO Address (ISA, MCA Modes) 0-07EB
Base Index Register (ISA, MCA Modes) 2
Direct Address (Coprocessor Mode) 0-08B

Registers LAW and LAR address register CPR. The cursor pattern RAM completes two 32x32 bit (or 4132 byte) planes, for a total of 128 bytes for each plane. A write or read to the CPR writes or reads the cursor pattern data

Bit #	RWD				D			
	7	6	5	4	3	2	1	0

Bit # Access Reset Description

7:0	RW	0	D	Cursor Pattern RAM Data
-----	----	---	---	-------------------------

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4.4 Video, Graphics, and Cursor Control

4.4.1 GSN Graphics Status Register

IO Address (ISA MCA Modem) 007FEA
Base Index Register (ISA MCA Modem) 2
Direct Address (Compressor Mode) 0000

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.4.2 Video, Graphics, and Cursor Control

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

4.4.3 Video, Graphics, and Cursor Control

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

0-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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4.4.4 Video, Graphics, and Cursor Control

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

01	Green is specified
10	Blue is specified

4.4.5 Video, Graphics, and Cursor Control

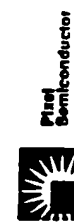
Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

CL 42017

Cirrus Confidential
Business Information

CL 42017
MicroDAC™



Pixel
Semiconductor

4.4.9 GFC Graphics Format Control

IO Address (ISA MCA Modem) 007FEC
Base Index Register (ISA MCA Modem) 2
Direct Address (Compressor Mode) 0000

Register GFC sets up the graphic interface timing and color format controls.

RD*	OFF		TC	CF	MA	TE	PD
1	0	0	4	3	3	1	0

4.4.10 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

4.4.11 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

4.4.12 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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4.4.13 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.4.14 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.4.15 Access Register

Read only register GSN is a module 3 counter. It sets up and monitors the CL 42017's status and IO cycles.

RD*	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	



Pixel Semiconductor

CL 42018
MediaDAC™

0.5 16-bit Color Sample Counter

0.5 16-bit Color Sample Counter
0.5 16-bit Color Sample Counter
0.5 16-bit Color Sample Counter
0.5 16-bit Color Sample Counter

Register CCR selects cursor modes and registers palette indexing for 16-bit graphics data modes and clock selection.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	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4.5.3 VGR Video Gamma Correction Mode

IO Address: (ISA MCA Mode) 007F0
Base Index Register: (ISA MCA Mode) 8
Direct Address: (Coprocessor Mode) 0017

The VGR pin is an 8-bit write port to the graphics color palette (a 24x24 bit memory array) and must be exercised in real time for each palette color.

For write operations:

- The first read operation reads the red 8-bit component of the palette color specified by VGR.
- The second read operation reads the green 8-bit component of the palette color specified by VGR.
- The third read operation reads the blue 8-bit component of the palette color specified by VGR.
- After the blue component is read, register VGR automatically increments to the next palette color. When the 8-bit write data is sent to the two 8-bit write ports, the data is stored with the next palette color.

For write operations:

- The first write operation writes the red 8-bit component of the palette color specified by VGR.
- The second write operation writes the green 8-bit component of the palette color specified by VGR.
- The third write operation writes the blue 8-bit component of the palette color specified by VGR.
- After the blue component is written, register VGR automatically increments to the next palette color.

7	6	5	4	3	2	1	0

Bit 0 Access Reset Description

70	R/W	0	D	Video gamma correction data

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4.5.3 VGR Video Gamma Address Read

IO Address: (ISA MCA Mode) 007F8
Base Index Register: (ISA MCA Mode) 8
Direct Address: (Coprocessor Mode) 0017

Register VGR is a modulo-256 counter that specifies the next 24-bit video gamma palette color to be read on the next read operation to register VGR. VGR specifies the same palette color for read cycles R, G, and B. After the read cycle B, it automatically increments by one to specify the next palette color.

7	6	5	4	3	2	1	0

Bit 0 Access Reset Description

70	R/W	0	RA	Read Address: Byte address of gamma palette RAM

4.6 Graphics Overlay Control

The graphics overlay controls comprise:

- an 8-bit Graphics Overlay Opcode — register GOC;
- a 32-bit Graphics Chroma Key — registers GCK;
- a 32-bit Graphics Key Mask — registers GKM;
- an 8-bit multiplexer.

The CL-PI2000 can be viewed as a dual-image formatter. The graphics image is in front, the video image is in back.

Every graphics pixel is either opaque or transparent.

- If the graphics pixel is opaque, its graphics color information is displayed on the screen.
- If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics pixels are transparent, based on a combination of two overlay control features:

- a TAG bit component in the video pixel data, which is generated outside the CL-PI2000;
- the graphics COLOR key switch, which is generated by ANDing the graphics pixel data with the GKM register, then comparing the results against the GCK register.



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4.6.1 GCR: Graphics Overlay Control

IO Address	(ISA MCA Model)	0-7F (F)
Base Index Register	(ISA MCA Model)	4
Direct Address	(Capacitance Mode)	0-11

GCR is an 8-bit value that inputs to an 8-bit multiplexer. The select signals to the multiplexer — the TAG bit and the graphics COI bit — determine which of the eight bits become the transparency control for each pixel line. A high bit in register GCR enables video and makes graphics transparent. The value selects the graphics path and ignores video input stream.

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Bit 0 Access Reset Description

IO	RW	0	1	Description
7	0	0	1	Transparency (Graphics path transparency control bit-map for TAG)
		0	1	Bit 0 value selects function
		0	1	Bit 0 value selects function

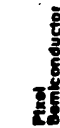
Table 5.2 GCR: Graphics Overlay Control

TAG	COI	0	1	2	3	4	5	6	7
0	0	0	10						
0	1	11							
1	0	12							
1	1	13							
0	0	14							
0	1	15							
1	0	16							
1	1	17							

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4.6.2 GCR: Graphics Overlay Control

IO Address	(ISA MCA Model)	0-7F (F)
Base Index Register	(ISA MCA Model)	4
Direct Address	(Capacitance Mode)	0-11

Registers GCR, GCR0, and GCR1 control the Graphics Overlay Control function. When the CL-PX2000 uses the 8-bit VGA port for graphics data, the data in register GCR is compared against four adjacent graphics pixels. GCR is compared to the least significant pixel by the PCLK SCLK ratio.

4.6.2.1 GCR: Graphics Overlay Control

7	6	5	4	3	2	1	0
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Bit 0 Access Reset Description

IO	RW	0	1	Description
7	0	0	1	Transparency (Graphics path transparency control bit-map for TAG)
		0	1	Bit 0 value selects function
		0	1	Bit 0 value selects function

4.6.2.2 GCR: Graphics Overlay Control

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Bit 0 Access Reset Description

IO	RW	0	1	Description
7	0	0	1	Transparency (Graphics path transparency control bit-map for TAG)
		0	1	Bit 0 value selects function
		0	1	Bit 0 value selects function

4.6.2.3 GCR: Graphics Overlay Control

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Bit 0 Access Reset Description

IO	RW	0	1	Description
7	0	0	1	Transparency (Graphics path transparency control bit-map for TAG)
		0	1	Bit 0 value selects function
		0	1	Bit 0 value selects function



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4.6.3 Graphics Key Mask

IO Address	(ISA MCA Modem)
Base Index Register	(ISA MCA Modem)
Device Address	(Capromem Mode)
047EC (R/W) Graphics Key Mask Red	
047ED (R/W) Graphics Key Mask Green	
047EE (R/W) Graphics Key Mask Blue	
047EF (R/W) Graphics Key Mask Mask	
047F0 (R/W) Graphics Key Mask Mask	
047F1 (R/W) Graphics Key Mask Mask	
047F2 (R/W) Graphics Key Mask Mask	
047F3 (R/W) Graphics Key Mask Mask	
047F4 (R/W) Graphics Key Mask Mask	
047F5 (R/W) Graphics Key Mask Mask	
047F6 (R/W) Graphics Key Mask Mask	
047F7 (R/W) Graphics Key Mask Mask	
047F8 (R/W) Graphics Key Mask Mask	
047F9 (R/W) Graphics Key Mask Mask	
047FA (R/W) Graphics Key Mask Mask	
047FB (R/W) Graphics Key Mask Mask	
047FC (R/W) Graphics Key Mask Mask	
047FD (R/W) Graphics Key Mask Mask	
047FE (R/W) Graphics Key Mask Mask	
047FF (R/W) Graphics Key Mask Mask	

Registers GRAM, GRAM, and GRAM control the Graphics Color Key Mask function.

- When the CL PX2080 uses the 8 bit VGA port for graphics data, the data in registers GRAM is ANDed with four adjacent graphics pixels. GRAM is compared to the most significant pixel by the PCIR (CLK) ring.
- When the CL PX2080 uses the 32 bit graphics port, the data in registers GRAM is used as specified by the PCIR (CLK) ring.

4.6.3.1 GRAM Graphics Key Mask Red

Access	Reset	Description
7	0	0
6	0	0
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0

70 RW 1 M8 Mask Red

4.6.3.2 GRAM Graphics Key Mask Green

Access	Reset	Description
7	0	0
6	0	0
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0

70 RW 1 M8 Mask Green

4.6.3.3 GRAM Graphics Key Mask Blue

Access	Reset	Description
7	0	0
6	0	0
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0

70 RW 1 M8 Mask Blue

70 RW 1 M8 Mask Blue

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4.7 Cursor Positioning

4.7.1 CTR: Cursor X Position

IO Address	(ISA MCA Modem)
Base Index Register	(ISA MCA Modem)
Device Address	(Capromem Mode)
042EC (R/W) Cursor X Position, Low Byte	
042ED (R/W) Cursor X Position, High Byte	
042EE (R/W) Cursor X Position, Low Byte	
042EF (R/W) Cursor X Position, High Byte	
042F0 (R/W) Cursor X Position, Low Byte	
042F1 (R/W) Cursor X Position, High Byte	
042F2 (R/W) Cursor X Position, Low Byte	
042F3 (R/W) Cursor X Position, High Byte	
042F4 (R/W) Cursor X Position, Low Byte	
042F5 (R/W) Cursor X Position, High Byte	
042F6 (R/W) Cursor X Position, Low Byte	
042F7 (R/W) Cursor X Position, High Byte	
042F8 (R/W) Cursor X Position, Low Byte	
042F9 (R/W) Cursor X Position, High Byte	
042FA (R/W) Cursor X Position, Low Byte	
042FB (R/W) Cursor X Position, High Byte	
042FC (R/W) Cursor X Position, Low Byte	
042FD (R/W) Cursor X Position, High Byte	
042FE (R/W) Cursor X Position, Low Byte	
042FF (R/W) Cursor X Position, High Byte	

8 bit registers CTR and CTR specify the X position of the bottom right corner of the cursor relative to the left side of the display screen.

- When CTR = 1 and CTR = 0, the right most column of pixels of the cursor is positioned at the left most column of pixels of the display screen.
- When CTR = 0 and CTR = 0, the cursor is positioned completely off screen one column to the left of the first displayed column of pixels on the screen.
- During reset, CTR=0x00 and CTR=0x00; the cursor is positioned in the upper left corner of screen.

4.7.1.1 CTR: Cursor X Position, Low Byte

Access	Reset	Description
7	0	0
6	0	0
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0

70 RW 0 X X position

4.7.1.2 CTR: Cursor X Position, High Byte

Access	Reset	Description
7	0	0
6	0	0
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0

70 RW 0 X X position

70 RW 0 X X position

70 RW 0 X X position

70 RW 0 X X position

70 RW 0 X X position

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4.2.2 CxY Cursor Y Position

IO Address: (ISA, MCA Mode) 0471A (CxY) Cursor Y Position (Low Byte)
Base Index Register: (ISA, MCA Mode) 0471B (CxY) Cursor Y Position (High Byte)
Data Address: (ISA, MCA Mode) 31C7A (CxY) Cursor Y Position (Low Byte)
Data Address: (ISA, MCA Mode) 31C7B (CxY) Cursor Y Position (High Byte)
Data Address: (ISA, MCA Mode) 0471C (CxY) Cursor Y Position (Low Byte)
Data Address: (ISA, MCA Mode) 0471D (CxY) Cursor Y Position (High Byte)

Registers CxY specify the Y position of the bottom right corner of the cursor relative to the top of the display screen.

- When CxY = 1 and CxY = 0, the bottom row of pixels of the cursor is positioned at the top row of pixels of the display screen.
- When CxY = 0 and CxY = 0, the cursor is positioned completely off screen, one column above the first displayed row of pixels on the screen.
- During reset CxY = 0 and CxY = 0, the cursor is positioned in the upper left corner of screen.

4.2.3 CxY Cursor Y Position, Low Byte

Bit	Access	Reset	Description
7	R/W	0	Y position
6	R/W	0	Y position
5	R/W	0	Y position
4	R/W	0	Y position
3	R/W	0	Y position
2	R/W	0	Y position
1	R/W	0	Y position
0	R/W	0	Y position

Bit 0 Access Reset Description

70 RW 0 Y Y position

4.2.4 CxY Cursor Y Position, High Byte

Bit	Access	Reset	Description
7	R/W	0	Y position
6	R/W	0	Y position
5	R/W	0	Y position
4	R/W	0	Y position
3	R/W	0	Y position
2	R/W	0	Y position
1	R/W	0	Y position
0	R/W	0	Y position

Bit 0 Access Reset Description

70 RW 0 0

30 RW 0 Y Y position

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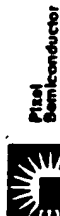
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4.2.5 VTC Video Format Control

IO Address: (ISA, MCA Mode) 047EC
Base Index Register: (ISA, MCA Mode) 4
Data Address: (ISA, MCA Mode) 0410

Register VTC sets up the video bus interface timing and color format controls.

Bit	Access	Reset	Description
7	R/W	0	OE*
6	R/W	0	OE*
5	R/W	0	OE*
4	R/W	0	OE*
3	R/W	0	OE*
2	R/W	0	OE*
1	R/W	0	OE*
0	R/W	0	OE*

Bit 0 Access Reset Description

70 RW 000 RSVD Reserved (write as zero)

4 RW 0 OE* Gamma Enable Enables the gamma LUTs

30 RW 0000 CSF Color Space Format of Video Bus:
0000 YUYV 4:2:2 format Non tagged data
0001 YUYV 4:2:2 format Non tagged data
0010 RGB 4:4:4 format
0011 RGB 4:4:4 format
0100 RGB 4:4:4 format
0101 RGB 4:4:4 format
0110 RGB 4:4:4 format (tag data)
0111 RGB 4:4:4 format (tag data)
1000 RGB 4:4:4 format (tag data)
1001 RGB 4:4:4 format (tag data)
1010 RGB 4:4:4 format (tag data)
1011 RGB 4:4:4 format (tag data)
1100 RGB 4:4:4 format (tag data)
1101 RGB 4:4:4 format (tag data)
1110 RGB 4:4:4 format (tag data)
1111 RGB 4:4:4 format (tag data)
All other bit configurations are reserved.

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6.0 Reserved Registers

0x0000	(16A MCA Mode)	0x0718 (RSV1 Reserved Register 1)
0x0001		0x0719 (RSV2 Reserved Register 2)
0x0002		0x071A (RSV3 Reserved Register 3)
0x0003		0x071B (RSV4 Reserved Register 4)
0x0004	(16A MCA Mode)	0x071C (RSV5 Reserved Register 5)
0x0005		0x071D (RSV6 Reserved Register 6)
0x0006		0x071E (RSV7 Reserved Register 7)
0x0007		0x071F (RSV8 Reserved Register 8)
0x0008	(Compressed Mode)	0x0720 (RSV9 Reserved Register 9)
0x0009		0x0721 (RSV10 Reserved Register 10)
0x000A		0x0722 (RSV11 Reserved Register 11)
0x000B		0x0723 (RSV12 Reserved Register 12)
0x000C		0x0724 (RSV13 Reserved Register 13)
0x000D		0x0725 (RSV14 Reserved Register 14)

Registers RSV1, RSV2, RSV3, and RSV4 are reserved.

Bit	Access	Reset	Description
7:0	R/W	0x	RSVD Reserved (write no reset)

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5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Storage Temperature -55°C to +150°C
Voltage on any pin with respect to ground 0.5 Volts to VDD + 0.5 Volts
Power Supply Voltage 0.5 Volts to VDD + 0.5 Volts
Lead Temperature (10 seconds) 260°C

5.2 CL-PI2080 DC Specifications (Digital)

Symbol	Parameter	MIN	MAX	Units	Conditions
VDD	Power Supply Voltage	4.75	6.25	V	Normal Operation
VIL	Input Low Voltage	0	0.8	V	
VOL	Output Low Voltage	2.0	VDD + 0.8	V	
VIL	Input High Voltage	2.4	0.4	V	VOL = 4 mA
VOL	Output High Voltage	2.4	0.4	V	IOL = 400 µA
VIL	Input Low Voltage CMOS	0.8	0.8	V	
VOL	Output Low Voltage CMOS	0.8	0.8	V	
VIL	Input High Voltage CMOS	0.4	0.4	V	VOL = 3.2 mA
VOL	Output High Voltage CMOS	3.6	0.4	V	IOL = 3.2 mA
IDD	Digital Supply Current		10	mA	VDD = 5.0V, Monitor
IOUT	Total Supply Current		10	mA	Note 1
I	Input Leakage	-10	10	µA	0 < VDD < VDD
CI	Input Capacitance		10	pF	
COU	Output Capacitance		10	pF	

NOTE: 1) IOUT is the sum of IDD + DACIOL + CLILVDD. IOUT must be < 200mA (package constraint).
2) DACIOL must not exceed VDD.



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5.3 CL-PX2080 DC Specifications (RAMDAC)

$V_{DD} = 5V \pm 5\%$, $I_o = 0$ to 100 unless otherwise specified

Symbol	Parameter	Min	Max	Units	Conditions
DAC VDD	Power Supply Voltage	4.75	5.25	V	Normal Operation
I_{DD}	DAC Reference Current	7.0	10.0	mA	Notes 1, 2
DAC I _{DD}	DAC Supply Current		75	mA	Note 3

NOTE: 1) Reference Current outside the specified limits may cause the analog outputs to become biased.
2) The Data Chart must be stable for a period of 10⁶ s after power up before proper DAC operation is guaranteed.
3) T₁ and T₂ are specified with the three analog outputs (A, B, C) each loaded with 37.5 ohms.

5.4 CL-PX2080 DAC Characteristics

$V_{DD} = 5V \pm 5\%$, $I_o = 0$ to 100 unless otherwise specified

Symbol	Parameter	Min	Max	Units	Conditions
R	Resolution	8		bits	
I_{DD}	Output Current		21	mA	$V_O = 1V$
C _o	Output Capacitance		12	pF	Between V_{IL} and V_{IH}
t_p	Analog Output Delay		30	ns	Notes 1, 2, 3
t_g	Analog Output Rise/Fall at 100%		5	ns	Note 2, 3, 4
t_s	Analog Output Settling time		15	ns	Note 2, 3, 5
I_{DC}	Analog Output Stare		600	ns	Note 2, 3, 6
FT	Clock and Data Feedthrough		30	dB	Note 2, 3, 8
DT	DAC to DAC Variability		± 2	%	Note 8, 7
DI	Glitch Immunity		75	pV and	Note 2, 3, 9
CT	DAC to DAC Crosstalk		-25	dB	Note 2, 3, 8

NOTE: 1) t_p is measured from the 50% point of VDDCK to 80% point of full scale transition.
2) Load is 37.5 ohms and 30 pF per analog output.
3) I_{DD} = 8.8 mA.
4) t_g is measured from 10% to 90% full scale.
5) t_s is measured from 50% point of full scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid point of the distribution of the three DACs measured at full scale deflection.

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5.5 AC Characteristics/Timing Information

This section includes system timing requirements for the CL-PX2080. Timings are provided in nanoseconds (ns) at TTL input levels with the ambient temperature varying from 0 to 70°C, and V_{CC} varying from 4.75 to 5.25V DC.

NOTE: 1) All timings assume a load of 30 pF.
2) TTL signals are measured at TTL threshold. CMOS signals are measured at CMOS threshold.

5.5.1 Index of Timing Information

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5.5.14	IO Timing (MCA Bus)	89
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5.5.34	IO Timing (MCA Bus)	89
5.5.35	IO Timing (MCA Bus)	89
5.5.36	IO Timing (MCA Bus)	89
5.5.37	IO Timing (MCA Bus)	89
5.5.38	IO Timing (MCA Bus)	89
5.5.39	IO Timing (MCA Bus)	89
5.5.40	IO Timing (MCA Bus)	89
5.5.41	IO Timing (MCA Bus)	89
5.5.42	IO Timing (MCA Bus)	89
5.5.43	IO Timing (MCA Bus)	89
5.5.44	IO Timing (MCA Bus)	89
5.5.45	IO Timing (MCA Bus)	89
5.5.46	IO Timing (MCA Bus)	89
5.5.47	IO Timing (MCA Bus)	89
5.5.48	IO Timing (MCA Bus)	89
5.5.49	IO Timing (MCA Bus)	89
5.5.50	IO Timing (MCA Bus)	89
5.5.51	IO Timing (MCA Bus)	89
5.5.52	IO Timing (MCA Bus)	89
5.5.53	IO Timing (MCA Bus)	89
5.5.54	IO Timing (MCA Bus)	89
5.5.55	IO Timing (MCA Bus)	89
5.5.56	IO Timing (MCA Bus)	89
5.5.57	IO Timing (MCA Bus)	89
5.5.58	IO Timing (MCA Bus)	89
5.5.59	IO Timing (MCA Bus)	89
5.5.60	IO Timing (MCA Bus)	89
5.5.61	IO Timing (MCA Bus)	89
5.5.62	IO Timing (MCA Bus)	89
5.5.63	IO Timing (MCA Bus)	89
5.5.64	IO Timing (MCA Bus)	89
5.5.65	IO Timing (MCA Bus)	89
5.5.66	IO Timing (MCA Bus)	89
5.5.67	IO Timing (MCA Bus)	89
5.5.68	IO Timing (MCA Bus)	89
5.5.69	IO Timing (MCA Bus)	89
5.5.70	IO Timing (MCA Bus)	89
5.5.71	IO Timing (MCA Bus)	89
5.5.72	IO Timing (MCA Bus)	89
5.5.73	IO Timing (MCA Bus)	89
5.5.74	IO Timing (MCA Bus)	89
5.5.75	IO Timing (MCA Bus)	89
5.5.76	IO Timing (MCA Bus)	89
5.5.77	IO Timing (MCA Bus)	89
5.5.78	IO Timing (MCA Bus)	89
5.5.79	IO Timing (MCA Bus)	89
5.5.80	IO Timing (MCA Bus)	89
5.5.81	IO Timing (MCA Bus)	89
5.5.82	IO Timing (MCA Bus)	89
5.5.83	IO Timing (MCA Bus)	89
5.5.84	IO Timing (MCA Bus)	89
5.5.85	IO Timing (MCA Bus)	89
5.5.86	IO Timing (MCA Bus)	89
5.5.87	IO Timing (MCA Bus)	89
5.5.88	IO Timing (MCA Bus)	89
5.5.89	IO Timing (MCA Bus)	89
5.5.90	IO Timing (MCA Bus)	89
5.5.91	IO Timing (MCA Bus)	89
5.5.92	IO Timing (MCA Bus)	89
5.5.93	IO Timing (MCA Bus)	89
5.5.94	IO Timing (MCA Bus)	89
5.5.95	IO Timing (MCA Bus)	89
5.5.96	IO Timing (MCA Bus)	89
5.5.97	IO Timing (MCA Bus)	89
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5.5.100	IO Timing (MCA Bus)	89

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5.5 IO Timing (ISA Bus)

Table 5-1 IO Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t ₁	Setup time valid address to $\overline{IOR}/\overline{OW}$ active			ns
t ₂	Delay $\overline{IOR}/\overline{OW}$ active to \overline{DEN} active \overline{DDIR} change			ns
t ₃	Delay \overline{IOR} active to data out bus 2			ns
t ₄	Delay \overline{IOR} active to data out valid			ns
t ₅	Pulse width $\overline{IOR}/\overline{OW}$			ns
t ₆	Delay $\overline{IOR}/\overline{OW}$ inactive to \overline{DEN} inactive \overline{DDIR} change			ns
t ₇	\overline{IOR} inactive to Tri-state delay			ns
t ₈	Address hold time from $\overline{IOR}/\overline{OW}$ active			ns
t ₉	Setup time data valid to \overline{CIW} inactive			ns
t ₁₀	Hold time \overline{CIW} inactive to data ready			ns
t ₁₁	Delay \overline{OW} inactive to read \overline{CIW} or \overline{QIR} active			ns
t ₁₂	Setup \overline{ACK} rising edge to \overline{OW} or \overline{QIR} active			ns
t ₁₃	Delay \overline{OW} or \overline{QIR} inactive to \overline{ACK} rising edge			ns

NOTE: 1) \overline{DEN} must be low

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NOTE: 2) The bus type address buffer enable must be qualified by \overline{DEN} to avoid data contention. See Section 3.1.1 on page 31 for additional information.

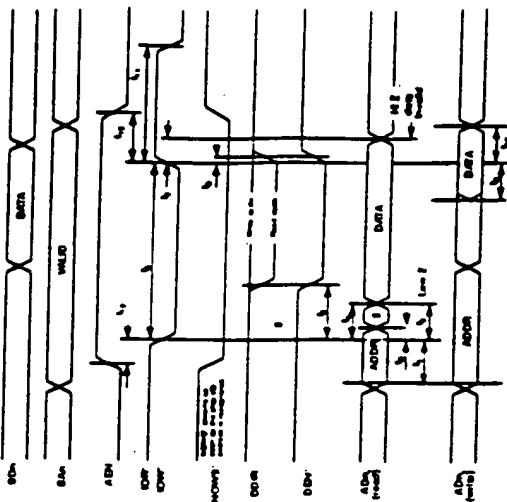


Figure 5-1 IO Timing, ISA Bus



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5.3.3 Timing (MCA Bus)

Table 5.3.3 CMD Timing (MCA Bus)

Symbol	Parameter	Unit	MAX	Unit
t ₁	Setup time address valid to CMD active	ns	80	ns
t ₂	Delay CMD active to DEN active	ns	80	ns
t ₃	Setup active setup to CMD active	ns	25	ns
t ₄	ADEN active setup to CMD active	ns	85	ns
t ₅	CMD pulse width	ns	25	ns
t ₆	Address hold from CMD active	ns	75	ns
t ₇	Status hold from CMD active	ns	75	ns

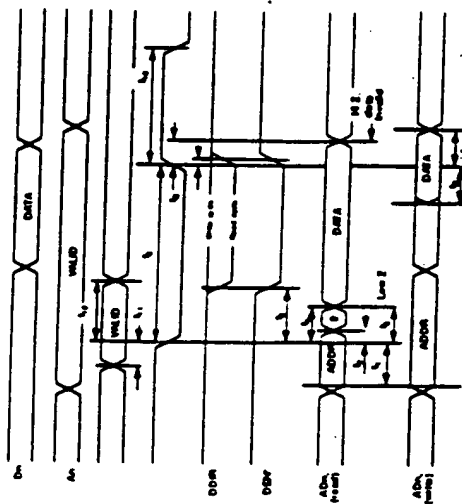
NOTE 1) See Write Cycle and Read Cycle diagrams for data timing with respect to CMD.



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Figure 5.3.3 CMD Timing (MCA Bus)



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Table 5.3 Clocks as Inputs (CLK = 1:1 Main Rate)

Symbol	Parameter	65 MHz		85 MHz		Unit
		MIN	MAX	MIN	MAX	
t_1	Rise time					ns
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_2	Fall time					ns
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_3	High Period (Note 1)					ns
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_4	Low Period (Note 1)					ns
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_5	Cycle time					ns
	PCLK0	15	18	15	18	ns
	PCLK1	11.5	15	11.5	15	ns
	LCLK	11.5	15	11.5	15	ns
	VCLK	20	20	20	20	ns

NOTE 1) LCLK and SCLK cycle and pulse width times are multiplied by 2.4 in 2:1, 4:1, 8:1 multiplying modes respectively

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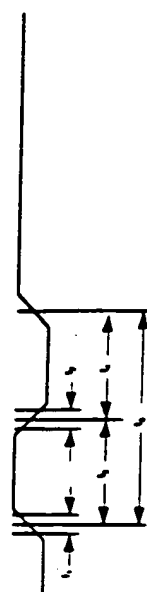


Figure 5.3 Clocks as Inputs
5.3.1 Syno, ROB, and QSD023 as Outputs Delay from PCLK0
Table 5.4 Syno, ROB, and QSD023 as Outputs Delay from PCLK0

Symbol	Parameter	85.03 MHz		85.03 MHz		Unit
		MIN	MAX	MIN	MAX	
t_1	PCLK0 rise to R.O.B output delay			20		ns
t_2	R.O.B output rise/fall			35		ns
t_3	R.O.B output full scale settling time			15/15		ns
t_4	PCLK0 rise to VSDOUT, HSOUT output delay			10		ns
t_5	PCLK0 rise to QSD023 output delay			20		ns
not shown						
not shown	R.O.B output to SENSE output delay			1		ns

NOTE: 1) Output delay is measured from the 50% point of the rising edge of PCLK0 to the 50% point of full scale transition.
2) Settling time is measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.
3) Output delay time is measured between the 10% and 90% points of full scale transition.
4) In 1:1 multiplying mode, ROB data is decoded and directly from LCLK and synchronizing with SCLK and PCLK is unnecessary and dependent. All timing PCLK references in table above apply to LCLK when 1:1 multiplying mode.



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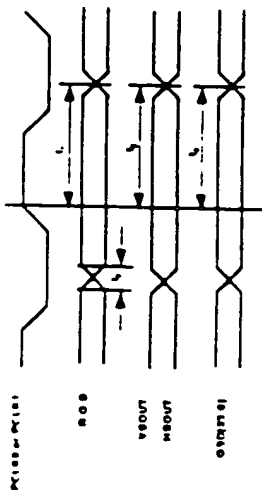


Figure 3.4 Sync, R.O.B, and OSTRIPn as Outputs Delay from PCLKn

3.5.0 Graphics Port Interface Timing
Table 3.5 Graphics Port Interface Timing

Symbol	Parameter	Unit	MAX	Unit
t_1	LCLK rise to SCLK rise synchronizer setup time	ns	4	ns
t_2	SCLK rise to LCLK rise synchronizer hold time	ns	0	ns
t_3	PCLKn rise to SCLK output delay	ns	10	ns
t_4	Graphics data, control to LCLK rise setup time	ns	4.0	ns
t_5	Graphics data, control to LCLK rise setup time	ns	0.2	ns
not shown	R.O.B output full scale settling time	ns	13/15	ns
not shown	R.O.B output to SENSE output delay	ns	1	ns
t_6	PCLK rise to VSOOUT HSOOUT output delay	ns	0	ns
t_7	PCLK rise to OSTRIPn output delay	ns	0	ns

NOTE: 1) SCLK timing relative to PCLK does not apply when in 1:1 multiplexing mode. In this mode, data is clocked in and out relative to LCLK and no synchronization is performed.

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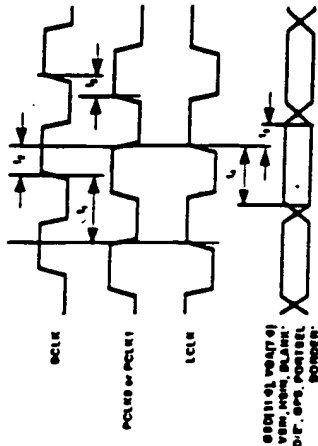


Figure 3.5 Graphics Port Interface Timing

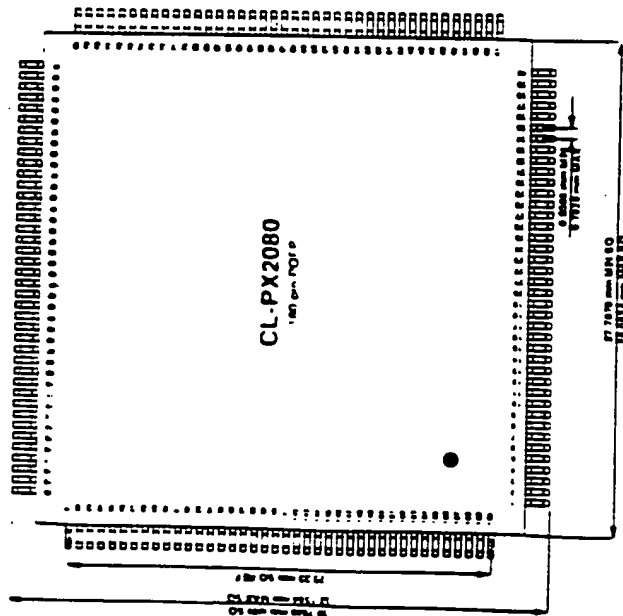
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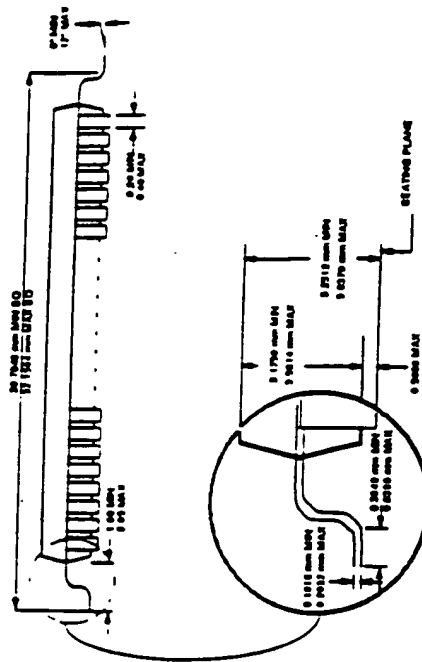


Figure 6-2. CL-PX2080 MediaDAC™ Package Information (Expanded View)

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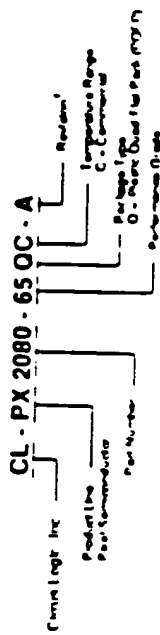
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7. ORDERING INFORMATION

When ordering the CL PX2080 use the following format:



* Contact Cirrus Logic for up to date information on this device

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